Proposed Draft

Serial ATA International Organization

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Serial ATA Technical Proposal # TP 030
Title : Gen1x, Gen2x Removal

This is an internal working document of the Serial ATA International Organization. As such, this is not a completed standard and has not been approved. The Serial ATA International Organization may modify the contents at any time. This document is made available for review and comment only.

Author Information

Author Name	Company	Email address
Charles Hill	Alta Engineering	cphill@altaeng.com

Workgroup Chair Information

Workgroup (Phy, Digital, etc…)	Chairperson Name	Email address
Phy	Charles Hill	cphill@altaeng.com

Document History

Version	Date	Comments
0	February 26, 2010	Initial release.
1	March 5, 2010	Remove f/1667 jitter rows in physical requirements table.
2	March 12, 2010	Don't delete footnote for mathematical TCTF for Gen3i (see other ECN)
3	June 21, 2010	Mark sections exclusive to Gen1x 2x as obsolete.

Introduction

The Gen1x and Gen2x electrical and mechanical specification was originally intended to address the interoperability between Serial ATA and Serial Attached SCSI (SAS) systems. The electrical parameters were in line with the corresponding SAS parameters. Over time, it has emerged that this interoperability need has been met in other ways. Since these specifications were added, there have been changes to the SAS specifications. At this point in time, either the Gen1x and Gen2x specifications need to be updated to be consistent with the SAS specification, or they need to be removed from the Serial ATA specification. There has been little or no interest in Gen1x or Gen2x. Therefore, this proposal removes Gen1x and Gen2x from the Serial ATA specification.

1 Technical Specification Changes

4.1.50 Gen1x (Obsolete)

The electrical specifications used in Long Backplane Applications and Data Center Applications supporting cable lengths up to and greater than two meters, defined at 1.5 Gbps.

4.1.54 Gen2x (Obsolete)

The electrical specifications used in Long Backplane Applications and Data Center Applications supporting cable lengths up to and greater than two meters, defined at 3.0 Gbps.

5.2 Usage Models

This section describes some of the potential applications of Serial ATA, including usage models that take advantage of features such as Native Command Queuing, enclosure management, Port Multipliers, and Port Selectors. Table 1 outlines the different usage models described throughout the section as well as highlights the relative requirements applicable to those usage models. Table 1 shows which characteristics in the first column are necessary to support the usage models in the top row.

Feature specific (FS) is intended to indicate that Gen1 is required but higher data rates are optional.

NOTE: The exact position of compliance points associated with the transmitter and the receiver are defined in sections 7.2.2.4 and 7.2.2.5.

Table 1 – Usage Model Descriptions

Characteristic	Internal 1 meter Cabled Host to Device	Short Backplane to Device	~~Long Back plane to Device~~	Internal 4-lane Cabled Disk Arrays	System to System Inter connects – Data Center Applications xSATA	~~System to System Inter connects – Data Center Applications xSATA~~	System to System Inter connects – External Desktop Applications eSATA	Proprietary Serial ATA Disk Arrays	Serial ATA and SAS	LIF-SATA
Use model section number	**Error! Reference source not found.**	**Error! Reference source not found.**	~~0~~	**Error! Reference source not found.**	0	~~0~~	**Error! Reference source not found.**	**Error! Reference source not found.**	**Error! Reference source not found.**	0
Cable and/or backplane type	Int SL	BP	~~BP~~	Int ML	Ext ML	~~Ext ML~~	Ext SL	BP and cable	BP	P
Cable length	<= 1 m			<= 1 m	<= 2 m	~~*subject to electrical requirements~~	<= 2 m			P
Cable Electrical	**Error! Reference source not found.**	P	~~P~~	**Error! Reference source not found.**	**Error! Reference source not found.**	~~Table 2~~	**Error! Reference source not found.**	**Error! Reference source not found.**	P	**Error! Reference source not found.**
Attenuation at 4.5GHz	-6dB	P	~~-16dB~~	-6dB	-8dB	~~-16dB~~	-8dB	-6dB	P	-6dB

Characteristic	Internal 1 meter Cabled Host to Device	Short Backplane to Device	~~Long Back plane to Device~~	Internal 4-lane Cabled Disk Arrays	System to System Inter connects – Data Center Applications xSATA	~~System to System Inter connects – Data Center Applications xSATA~~	System to System Inter connects – External Desktop Applications eSATA	Proprietary Serial ATA Disk Arrays	Serial ATA and SAS	LIF-SATA
Host-side connector	**Error! Reference source not found.**	P	~~P~~	**Error! Reference source not found.** or **Error! Reference source not found.**	**Error! Reference source not found.** (key 7)	~~**Error! Reference source not found.** or **Error! Reference source not found.** (key 1)~~	**Error! Reference source not found.**	**Error! Reference source not found.** or P	SAS	**Error! Reference source not found.**
Device-side connector	**Error! Reference source not found.**	**Error! Reference source not found.**	~~**Error! Reference source not found.** (inside canister)~~	**Error! Reference source not found.**	**Error! Reference source not found.** (key 7)	~~**Error! Reference source not found.** or **Error! Reference source not found.** (key 1 or 4)~~	**Error! Reference source not found.**	**Error! Reference source not found.**	**Error! Reference source not found.**	**Error! Reference source not found.**
Gen1i 1.5 Gbps	R	D (host to provide received signal)	~~D~~	R	NS	~~NS~~	NS	R	D	R
Gen1m 1.5 Gbps	NS	H	~~NS~~	NS	R (key 7)	~~NS~~	R	NS	NS	NS
Gen2i 3.0 Gbps	FS	D (host to provide received signal)	~~D~~	FS	NS	~~NS~~	NS	FS	D	FS

Characteristic	Internal 1 meter Cabled Host to Device	Short Backplane to Device	~~Long Back plane to Device~~	Internal 4-lane Cabled Disk Arrays	System to System Inter connects – Data Center Applications xSATA	~~System to System Inter connects – Data Center Applications xSATA~~	System to System Inter connects – External Desktop Applications eSATA	Proprietary Serial ATA Disk Arrays	Serial ATA and SAS	LIF-SATA
Gen2m 3.0 Gbps	NS	H	~~NS~~	NS	FS (key 7)	~~NS~~	FS	NS	NS	NS
~~Gen1x 1.5 Gbps~~	~~NS~~	~~NS~~	~~H, D~~	~~NS~~	~~NS~~	~~R~~	~~NS~~	~~NS~~	~~NS~~	~~NS~~
~~Gen2x 3.0 Gbps~~	~~NS~~	~~NS~~	~~H, D~~	~~NS~~	~~NS~~	~~FS~~	~~NS~~	~~NS~~	~~NS~~	~~NS~~
Gen3i 6.0 Gbps	FS	NS	~~NS~~	FS	NS	~~NS~~	NS	FS	D	FS
Hot plug support	NS	R	~~R~~	NS	R	~~R~~	R	R	R	NS

Key:
R – Required : configuration requires appropriate capabilities
FS – Feature specific : configuration is supported by specification but may be tied to an optional capability
NOTE: Feature specific is intended to indicate that Gen1 is required but higher data rates are optional.
NS – Not supported : configuration is not supported by definition in specification
P – Proprietary : implementation is vendor specific and not defined in specification
H – Host
D – Device
SL – single lane
ML – multi-lane
Int – Internal
Ext – External
BP – Backplane
NOTE : Many of the references in the table are section numbers or notations of clarification which do not require Key values

5.2.3 Long Backplane to Device (Obsolete)

~~In this 1.5 Gbps or 3.0 Gbps application, the length of the backplane is longer than in the previous example so attenuation of signals reduce their amplitude beyond usable levels. Therefore an IC may be placed between the device and the canister's connector to the backplane to convert the disk's Gen1i/Gen2i levels to Gen1x/Gen2x levels. A typical circuit might be a Serial ATA Port Selector. Likewise, the host controller complies with Gen1x/Gen2x levels at the backplane connector to the host controller. This allows reliable transmission of Serial ATA data over backplanes longer than in the Short Backplane Application described above. The burden of determining whether a Backplane Application is Short or Long falls upon the system designer based on the system's attenuation. Compliance points are located at the Serial ATA mated connectors on both the canister (Gen1x/Gen2x) and the host controller (Gen1x/Gen2x). The Gen1x/Gen2x Electrical Specifications require Hot Plug capability so that the disk/canister may be plugged and unplugged without damage.~~

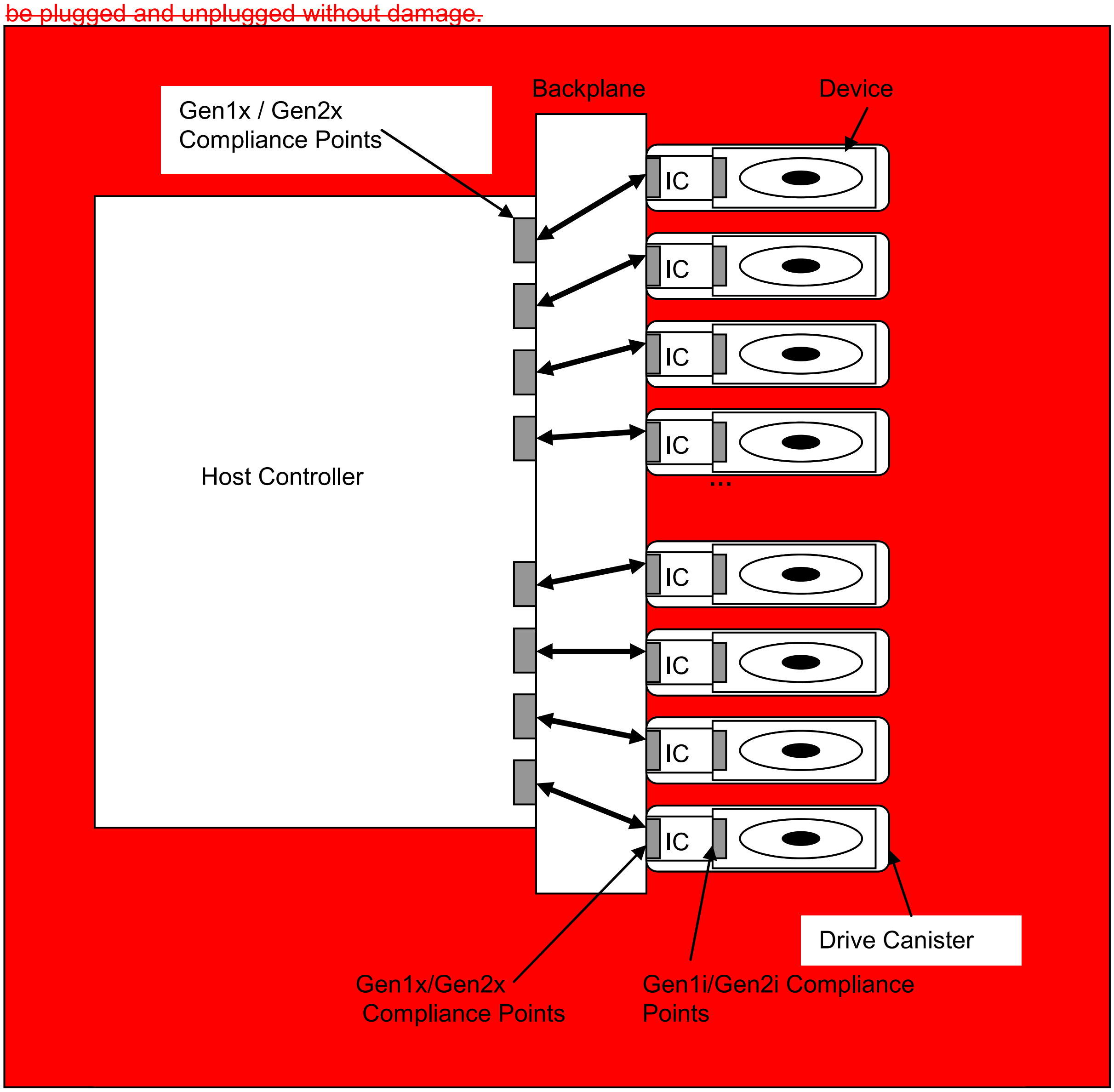


Figure 1 – ~~Long Backplane to Device Application~~

5.2.5 System-to-System Interconnects – Data Center Applications (xSATA)

This application is defined as external storage applications that require more than one serial link between systems. This application uses the external Multilane cables defined in sections **Error! Reference source not found.** and **Error! Reference source not found.**, and may be referred to as xSATA.

For system-to-system interconnects that require cables of approximately two meters or less (i.e. pedestal to pedestal, blade to blade, or intrarack connections) ~~either~~ Gen1m/Gen2m ~~or Gen1x/Gen2x Electrical Specifications are~~ is used. ~~For system-to-system interconnects that require distances greater than two meters (i.e. rack to rack,) Gen1x/Gen2x Electrical Specifications are used.~~

All external Serial ATA cables function at both 1.5 Gbps and 3.0 Gbps. Use of a cable that operates at 1.5 Gbps but not at 3.0 Gbps is allowed but this cable assembly shall not be interchangeable with standard Serial ATA cables. For example, if this 1.5 Gbps cable uses Serial ATA specified connectors, the cable shall be keyed to insure that it cannot plug into standard Serial ATA connections. Hot pluggability is a requirement in this application.

Compliance points are located at the mated bulkhead connectors of each system as shown in the example implementation in Figure 2. If a SATA endpoint device is included in the system, it shall not be connected directly to the external connectors. Instead, a bridge shall be used between the external connectors and the endpoint device. Some examples of bridges include repeaters/retimers, Port Multipliers, and RAID controllers.

~~NOTE: Interconnects between Gen1m/Gen2m and Gen1x/Gen2x systems are not allowed.~~

NOTE: Gen3 is not defined for xSATA.

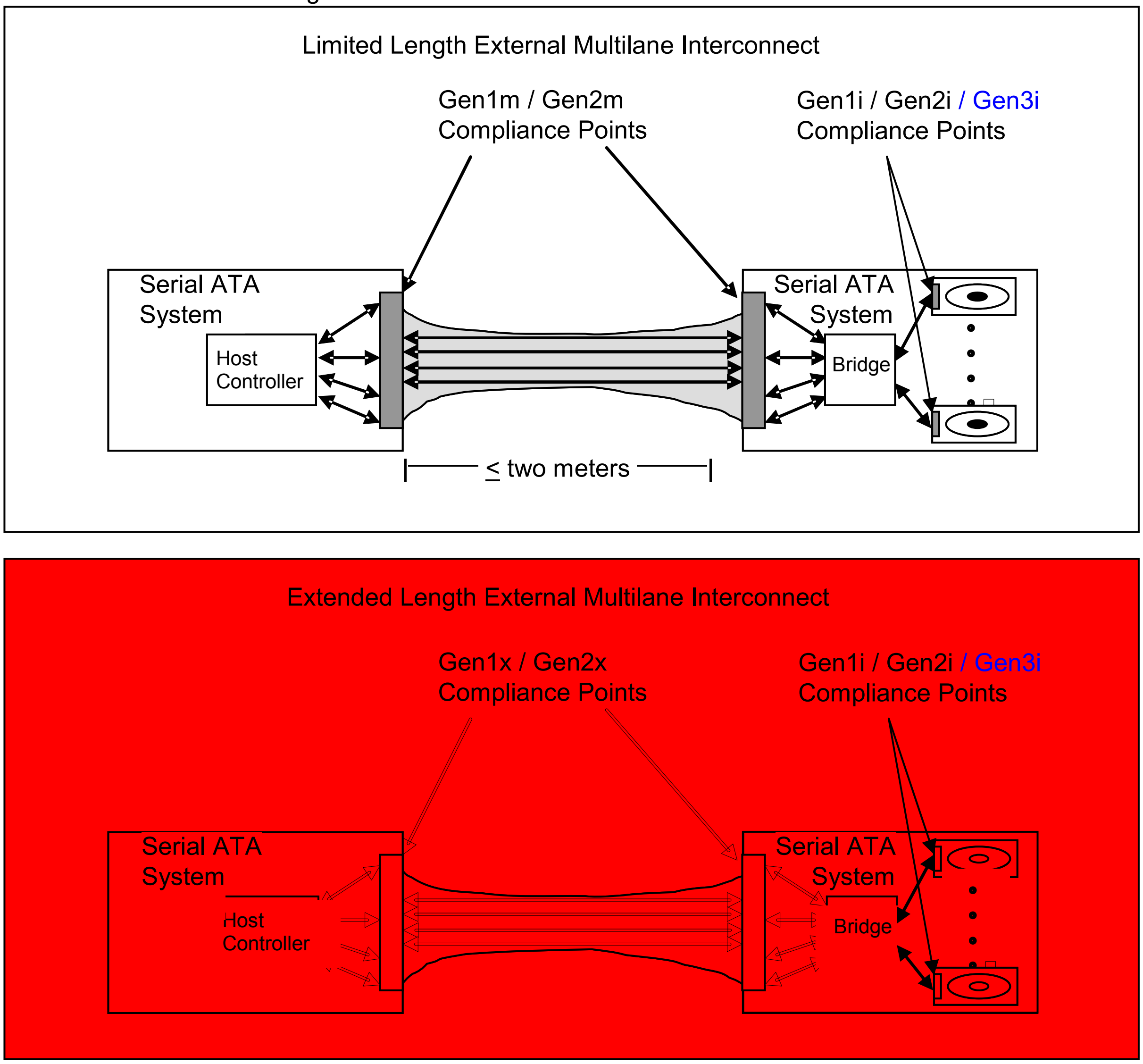


Figure 2 – System-to-System Data Center Interconnects

5.2.10 Mobile Applications

Applications and compliance points for Serial ATA devices within or connected to mobile computers are not defined in this document, except for embedded applications. If any proprietary cables/connectors or electrical specifications are developed for this application, the system shall be designed so as to prevent connection with standard SATA components. If standard cables/connectors/electrical interfaces are used within the mobile computer, within the docking bay or to external storage components, these shall comply with the applicable requirements in this specification and interoperate properly with Serial ATA components.

Internal Applications:

It is expected that all internal interfaces comply with the Gen1i, Gen2i, and/or Gen3i specifications. Any mobile computer designer modifying electrical specifications of hosts and devices within the mobile computer is free to do so, however, all proprietary interfaces shall be designed so as to prevent connection with standard SATA components.

Docking Bay Applications:
Proprietary docking bay interfaces shall be designed so as to prevent connection with standard SATA components.

External Applications:
Applications for external Serial ATA interfaces on mobile computers may use either the External Desktop cable/connector (Gen1m/Gen2m) or the System-to-System Data Center cable/connector (Gen1m/Gen2m ~~or Gen1x/Gen2x~~). Proprietary solutions shall be designed so as to prevent connection with standard SATA components.

6.5.2.1 Multilane Cable Conformance Criteria

The External Multilane cable/connector shall be used with Gen1m/Gen2m ~~and Gen1x/Gen2x~~ signal levels only. If Gen1m/Gen2m signal levels are used, the cable length is limited to two meters. ~~If Gen1x/Gen2x signal levels are used, cable lengths up to and greater than two meters are supported.~~

6.5.2.1.1 Electrical Parameters

The External Multilane cable assembly operating at Gen1m and Gen2m levels shall meet the electrical characteristics defined in **Error! Reference source not found.**.

~~The External Multilane cable assembly operating at Gen1x and Gen2x levels shall meet the electrical characteristics defined in Table 2.~~

6.5.3.1 Conformance Criteria

The External Multilane cable/connector shall be used with ~~either~~ Gen1m/Gen2m ~~or Gen1x/Gen2x~~ signal levels.

- 4 lanes, SAS/Serial ATA signals.
- Cable length is two meters maximum for Gen1m and Gen2m applications.
- ~~Cable length is up to and greater than two meters for Gen1x and Gen2x applications.~~
- RX, TX, RX, TX pin sequencing to minimize crosstalk.
- Ground reference between each pair.
- Performance for 3.0 Gbps.
- Keying features for "m" ~~and "x"~~ cables.

6.5.3.1.1 Electrical Parameters

The External Multilane cable assembly operating at Gen1m and Gen2m levels shall meet the electrical characteristics defined in **Error! Reference source not found.**.

~~The External Multilane cable assembly operating at Gen1x and Gen2x levels shall meet the electrical characteristics defined in Table 2.~~

6.6.1 Serial ATA Cable

6.6.1.1 Electrical Requirements

The electrical requirements for the internal single lane and Multilane Serial ATA cables and connectors for systems operating at Gen1i, Gen2i or Gen3i levels are listed in **Error! Reference source not found.**.

~~The electrical requirements for the External Multilane cable and connector for systems operating at Gen1x or Gen2x levels are defined in Table 2.~~

~~Table 2 – Table 21 Extended External Multilane Cable / Connector Measurement Parameter and Requirements~~

~~Parameter~~	~~Requirement~~	~~Procedure~~
~~Mated Connector Differential Impedance~~	~~100 Ohms ±10%~~	~~P1~~
~~Cable Absolute Differential Impedance~~	~~100 Ohms ±5%~~	~~P2~~
~~Cable Pair Matching Impedance~~	~~±5 Ohms~~	~~P3~~
~~Common Mode Impedance~~	~~25 Ohms - 40 Ohms~~	~~P4~~
~~Maximum Insertion Loss of Cable (10-4500 MHz)~~	~~16 dB~~	~~P5~~
~~Maximum Crosstalk: CXT (10-4500 MHz)~~	~~30 dB CXT~~	~~P7~~
~~Maximum Rise Time~~	~~150 ps (20-80%)~~	~~P8~~
~~Maximum Inter-Symbol Interference~~	~~60 ps~~	~~P9~~
~~Maximum Intra-Pair Skew~~	~~20 ps~~	~~P10~~

~~Note: All External Multilane cables longer than 2 meters use Gen1x or Gen2x levels.~~

7.1 Descriptions of Phy Electrical Specifications

The following terms have been developed for the various Electrical Specifications:

- **Gen1i**: Generation 1 Electrical Specifications: These are the 1.5 Gbps electrical specifications for internal host to device applications.
- **Gen1m**: Generation 1 Electrical Specifications for Short Backplane and external cabling applications: These are the 1.5 Gbps electrical specifications aimed at short 1.5 Gbps internal backplane applications, External Desktop Applications using the external single lane cable, and System-to-System Data Center Applications using external Multilane cables up to two meters in length. These include only modified receiver Differential input specifications. All other electrical specifications relating to Gen1m compliance points are identical to Gen1i specifications. This specification is for these limited applications only and is not intended for any other system topology.
- ~~**Gen1x**: Extended Length 1.5 Gbps Electrical Specifications: These are electrical specifications aimed at 1.5 Gbps links in Long Backplane and System-to-System Data Center Applications supporting external Multilane cables up to and greater than two meters. These specifications are based upon the SAS references.~~
- **Gen2i**: Generation 2 Electrical Specifications: These are 3.0 Gbps electrical specifications for internal host to device applications.
- **Gen2m**: Generation 2 Electrical Specifications for Short Backplane and External Desktop Applications: These are 3.0 Gbps electrical specifications aimed at short internal backplane applications, External Desktop Applications using the external single lane cable, and System-to-System Data Center Applications using external Multilane cables up to two meters in length. These include only modified receiver differential input specifications. All other electrical specifications relating to Gen2m compliance points are identical to Gen2i specifications. This specification is for this limited application only and is not intended for any other system topology.
- ~~**Gen2x**: Extended Length 3.0 Gbps Electrical Specifications: These are electrical specifications aimed at 3.0 Gbps links in Long Backplane and System-to-System Data Center Applications supporting external Multilane cables up to and greater than two meters. These specifications are based upon the SAS references.~~
- **Gen3i**: Generation 3 Electrical Specifications: These are 6.0 Gbps electrical specifications for internal host to device applications.

7.2.1 Physical Layer Requirements Tables

Table 3 – General Specifications

Parameters	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
Channel Speed	Gbps	Nom	1.5			3.0			6.0	**Error! Reference source not found.**	-
Fbaud	GHz	Nom	1.5			3.0			6.0	-	-
FER, Frame Error Rate		Max	8.2e-8 at 95% confidence level			8.2e-8 at 95% confidence level			8.2e-8 at 95% confidence level	**Error! Reference source not found.**	**Error! Reference source not found.**
T_{UI}, Unit Interval	ps	Min	666.4333			333.2167			166.6083	**Error! Reference source not found.**	**Error! Reference source not found.**
		Nom	666.6667			333.3333			166.6667		
		Max	670.2333			335.1167			167.5583		
f_{tol}, TX Frequency Long Term Accuracy	ppm of Fbaud	Min	-350			-350			-350	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max	+350			+350			+350		
f_{SSC}, Spread-Spectrum Modulation Frequency	kHz	Min	30			30			30	**Error! Reference source not found. Error! Reference source not found.**	**Error! Reference source not found.**
		Max	33			33			33		
SSC_{tol}, Spread-Spectrum Modulation Deviation	ppm of Fbaud	Min	-5350			-5350			-5350	**Error! Reference source not found. Error! Reference source not found.**	**Error! Reference source not found.**
		Max	+350			+350			+350		

Parameters	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$V_{cm,dc}$, DC Coupled Common Mode Voltage	mV	Min	200		-	(AC only)			(AC only)	0	0
		Nom	250		-	(AC only)			(AC only)		
		Max	450		-	(AC only)			(AC only)		
$V_{cm,ac\ coupled}$, AC Coupled Common Mode Voltage	mV	Min	0		-	-			-	0	**Error! Reference source not found.**
		Max	2000		-	-			-		
Z_{diff}, Nominal Differential Impedance	Ohm	Nom	100		-	-			100	**Error! Reference source not found.**	**Error! Reference source not found.**
$C_{ac\ coupling}$ AC Coupling Capacitance	nF	Max	12			12			12	0	**Error! Reference source not found.**
$t_{settle,cm}$, Common Mode Transient Settle Time	ns	Max	10		-	-			-	**Error! Reference source not found.**	**Error! Reference source not found.**
V_{trans}, Sequencing Transient Voltage	V	Min	-2.0			-2.0			-2.0	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max	2.0			2.0			2.0		

Table 4 – Transmitter Specifications

Parameters	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
V_{trans}, Sequencing Transient Voltage LL	V	Min	-			-			-1.2	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max	-			-			1.2		
Z_{diffTX}, TX Pair Differential Impedance	Ohm	Min	85		~~85~~	-		~~85~~	-	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max	115		~~115~~	-		~~115~~	-		
Z_{s-eTX}, TX Single-Ended Impedance	Ohm	Min	40		-	-			-	**Error! Reference source not found.**	**Error! Reference source not found.**

Parameters	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$RL_{DD11,TX}$, TX Differential Mode Return Loss (All Values Min)	dB	75 MHz-150MHz	14	14	-	-	-	-	-	Error! Reference source not found.	Error! Reference source not found.
		150 MHz-300 MHz	8	8	-	14	14	-	-		
		300 MHz-600 MHz	6	6	-	8	8	-	-		
		600 MHz-1.2 GHz	6	6	-	6	6	-	-		
		1.2 GHz-2.4 GHz	3	3	-	6	6	-	-		
		2.4 GHz-3.0 GHz	1	-	-	3	3	-	-		
		3.0 GHz-5.0 GHz	-	-	-	1	-	-	-		
$RL_{DD11,TX}$, TX Differential Mode Return Loss Start for slope	dB	Min at 300MHz	-			-	-	-	14	Error! Reference source not found.	Error! Reference source not found.
Slope of TX Differential Mode Return Loss	dB/dec	Nom	-			-	-	-	-13		
TX Differential Mode Return Loss Max Frequency	GHz	Max	-			-	-	-	3		

Parameters	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$RL_{CC11,TX}$, TX Common Mode Return Loss (all Values Min)	dB	150 MHz-300 MHz		-		8	5	-	-	Error! Reference source not found.	Error! Reference source not found.
		300 MHz-600 MHz		-		5	5	-	-		
		600 MHz-1.2 GHz		-		2	2	-	-		
		1.2 GHz-2.4 GHz		-		1	1	-	-		
		2.4 GHz-3.0 GHz		-		1	1	-	-		
		3.0 GHz-5.0 GHz		-		1	-	-	-		
$RL_{DC11,TX}$, TX Impedance Balance (all values Min)	dB	150 MHz-300 MHz		-		30	30	-	30	Error! Reference source not found.	Error! Reference source not found.
		300 MHz-600 MHz		-		20	20	-	30		
		600 MHz-1.2 GHz		-		10	10	-	20		
		1.2 GHz-2.4 GHz		-		10	10	-	10		
		2.4 GHz-3.0 GHz		-		4	4	-	10		
		3.0 GHz-5.0 GHz		-		4	-	-	4		
		5.0 GHz-6.5 GHz		-		-	-	-	4		

Table 5 – Transmitted Signal Requirements

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
V_{diffTX}, TX Differential Output Voltage	mVppd	Min	400	400	~~400~~	400	400	~~400~~	-	**Error! Reference source not found.**	0
		Min	-	-	-	-	-	-	240		**Error! Reference source not found.**
		Nom	500		-	-			-		0
		Max	600		~~1600~~	700		~~1600~~	-		
		Max	-		-	-		-	900		**Error! Reference source not found.**
UI_{VminTX}, TX Minimum Voltage Measurement Interval	UI		0.45-0.55		~~0.5~~	0.45-0.55		~~0.5~~	-	**Error! Reference source not found.**	0
			-		-	-		-	0.50		**Error! Reference source not found.**

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	**Gen1m**	**~~Gen1x~~**	**Gen2i**	**Gen2m**	**~~Gen2x~~**	**Gen3i**		
$t_{20\text{-}80TX}$, TX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		~~67 (.10)~~	67 (.20)			33 (0.20)	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max 20-80%	273 (.41)		~~273 (.41)~~	136 (.41)			68 (0.41)		
t_{skewTX}, TX Differential Skew	ps	Max	20			20		~~15~~	20	**Error! Reference source not found.**	**Error! Reference source not found.**
$V_{cm,acTX}$, TX AC Common Mode Voltage	mVp-p	Max	-			50		-	-	0	**Error! Reference source not found.**

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	**Gen1m**	**~~Gen1x~~**	**Gen2i**	**Gen2m**	**~~Gen2x~~**	**Gen3i**		
$V_{cm,acTX}$, TX AC Common Mode Voltage	dBmV (rms)	3 GHz Max	-		-	-		-	26	**Error! Reference source not found.**	**Error! Reference source not found.**
		6 GHz Max	-		-	-		-	30		
$D_{VdiffOOB}$, OOB Differential Delta	mV	Max	-		~~25~~	25			25	0	**Error! Reference source not found.**

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
D_{VcmOOB}, OOB Common Mode Delta	mV	Max	-		~~50~~	50			50	0	**Error! Reference source not found.**
R/F_{bal}, TX Rise/Fall Imbalance	%	Max	-		-	20		-	-	0	**Error! Reference source not found.**
Amp_{bal}, TX Amplitude Imbalance	%	Max	-		~~10~~	10			-	0	**Error! Reference source not found.**

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
TJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	0.37		-	0.37		-	-	0 Error! Reference source not found.	0 0
DJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	0.19		-	0.19		-	-		
Jitter Transfer Function Bandwidth (D24.3, high pass -3dB)	MHz	Min	1.1		-	1.1		-	-	Error! Reference source not found.	0
		Nom	2.1		-	2.1		-	-	Error! Reference source not found.	0
		Max	3.1		-	3.1		-	-	Error! Reference source not found.	0
Jitter Transfer Function Peaking	dB	Min	0		-	0		-	-	Error! Reference source not found.	0
		Nom	0		-	0		-	-	Error! Reference source not found.	0

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
		Max	3.5		-	3.5		-	-	Error! Reference source not found.	0
Jitter Transfer Function Low Frequency Attenuation	dB	Min	69		-	69		-	-	Error! Reference source not found.	0
		Nom	72		-	72		-	-	Error! Reference source not found.	0
		Max	75		-	75		-	-	Error! Reference source not found.	0
Jitter Transfer Function Low Frequency Attenuation Measurement Frequency	kHz		30±1%		-	30±1%		-	-	Error! Reference source not found.	0
Jitter Transfer Function Bandwidth (D24.3, high pass -3dB) (Gen3)	MHz	Min	-		-	-		-	2.2	Error! Reference source not found.	0
		Nom	-		-	-		-	4.2	Error! Reference source not found.	0

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
		Max	-		-	-		-	6.2	Error! Reference source not found.	0
Jitter Transfer Function Peaking (Gen3)	dB	Min	-		-	-		-	0	Error! Reference source not found.	0
		Nom	-		-	-		-	0	Error! Reference source not found.	0
		Max	-		-	-		-	3.5	Error! Reference source not found.	0
Jitter Transfer Function Low Frequency Attenuation (Gen3)	dB	Min	-		-	-		-	35.2	Error! Reference source not found.	0
		Nom	-		-	-		-	38.2	Error! Reference source not found.	0
		Max	-		-	-		-	41.2	Error! Reference source not found.	0

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x	Gen3i		
Jitter Transfer Function Low Frequency Attenuation Measurement Frequency (Gen3)	kHz		-		-	-		-	420 +/- 1%	**Error! Reference source not found.**	0
TJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.55	-		0.55	-	0 **Error! Reference source not found.**	0 0
DJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.35	-		0.35	-		
TJ before and after CIC, Clk-Data JTF Defined	UI	Max	-			-			RJ p-p meas. + 0.34	0 **Error! Reference source not found.**	0 **Error! Reference source not found.**
RJ before CIC, MFTP Clk-Data JTF Defined	UI	Max	-			-			0.18 p-p (2.14 ps 1 sigma)		

Table 6 – Receiver Specifications

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x	Gen3i		
Z_{diffRX} RX Pair Differential Impedance	Ohm	Min	85			-		~~85~~	-	**Error! Reference source not found.**	**Error! Reference source not found.**
		Max	115			-		~~115~~	-		
Z_{s-eRX} RX Single-Ended Impedance	Ohm	Min	40		-	-			-	**Error! Reference source not found.**	**Error! Reference source not found.**

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$RL_{DD11,RX}$, RX Differential Mode Return Loss (all values Min)	dB	75MHz-150MHz	18	18	-	-	-	-	-	Error! Reference source not found.	Error! Reference source not found.
		150 MHz-300 MHz	14	14	-	18	18	-	-		
		300 MHz-600 MHz	10	10	-	14	14	-	-		
		600 MHz-1.2 GHz	8	8	-	10	10	-	-		
		1.2 GHz-2.4 GHz	3	3	-	8	8	-	-		
		2.4 GHz-3.0 GHz	1	-	-	3	3	-	-		
		3.0 GHz-5.0 GHz	-	-	-	1	-	-	-		
$RL_{DD11,RX}$, RX Differential Mode Return Loss	dB	Min at 300MHz	-			-			18	Error! Reference source not found.	Error! Reference source not found.
Slope of RX Differential Mode Return Loss	dB/dec	Nom	-			-			-13		
RX Differential Mode Return Loss Max Frequency	GHz	Max	-			-			6.0		

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$RL_{CC11,RX}$, RX Common Mode Return Loss (all values Min)	dB	150 MHz-300 MHz	-			5	5	-	-	**Error! Reference source not found.**	**Error! Reference source not found.**
		300 MHz-600 MHz	-			5	5	-	-		
		600 MHz-1.2 GHz	-			2	2	-	-		
		1.2 GHz-2.4 GHz	-			1	1	-	-		
		2.4 GHz-3.0 GHz	-			1	1	-	-		
		3.0 GHz-5.0 GHz	-			1	-	-	-		

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
$RL_{DC11,RX}$, RX Impedance Balance (all values Min)	dB	150 MHz-300 MHz		-		30	30	-	30	**Error! Reference source not found.**	**Error! Reference source not found.**
		300 MHz-600 MHz		-		30	30	-	30		
		600 MHz-1.2 GHz		-		20	20	-	20		
		1.2 GHz-2.4 GHz		-		10	10	-	10		
		2.4 GHz-3.0 GHz		-		4	4	-	10		
		3.0 GHz-5.0 GHz		-		4	-	-	4		
		5.0 GHz-6.5 GHz		-		4	-	-	4		

Table 7 – Lab-Sourced Signal (for Receiver Tolerance Testing)

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
V_{diffRX}, RX Differential Input Voltage		Min	325	240	~~275~~	275	240	~~275~~	-	Error! Reference source not found.	Error! Reference source not found.
	mVppd	Min	-	-	-	-	-	-	240		Error! Reference source not found. Error! Reference source not found.
		Nom	400		-	-	-	-	-		Error! Reference source not found.
		Max	600		~~1600~~	750	750	~~1600~~	-		
		Max	-		-	-	-	-	1000		Error! Reference source not found. Error! Reference source not found.
$t_{20\text{-}80RX}$, RX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		~~67 (.10)~~	67 (.20)			-	Error! Reference source not found.	Error! Reference source not found.
			-		-	-			62 (0.37)		Error! Reference source not found. Error! Reference source not found.

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
		Max 20-80%	273 (.41)			136 (.41)			-		**Error! Reference source not found.**
			-			-			75 (0.45)		**Error! Reference source not found.** **Error! Reference source not found.**
UI_{VminRX}, RX Minimum Voltage Measurement Interval	UI		-		~~0.5~~	0.5			-	**Error! Reference source not found.**	**Error! Reference source not found.**
			-		~~-~~	-			0.5		**Error! Reference source not found.**
t_{skewRX}, RX Differential Skew	ps	Max	-		~~80~~	50		~~75~~	30	0	**Error! Reference source not found.**
$V_{cm,acRX}$, RX AC Common Mode Voltage	mVp-p	Max	100		~~150~~	100		~~150~~	100	0	0
$f_{cm,acRX}$, AC Common Mode Frequency	MHz	Min	2			2			2	**Error! Reference source not found.**	0
		Max	200			200			200		

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
TJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	0.60			0.60		-	-		
DJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	0.42			0.42		-	-		

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
~~TJ at Connector, Clk-Data, f_{BAUD}/1667~~	~~UI~~	~~Max~~	~~-~~		~~0.65~~	~~-~~		~~0.65~~	~~-~~	~~0 Error! Reference source not found.~~	~~0~~ ~~0~~
~~DJ at Connector, Clk-Data, f_{BAUD}/1667~~	~~UI~~	~~Max~~	-		~~0.35~~	-		~~0.35~~	-		
TJ after CIC, Clk-Data JTF Defined	UI	Max	-		~~-~~	-		~~-~~	0.60	0 Error! Reference source not found.	0 Error! Reference source not found.
RJ before CIC, MFTP Clk-Data JTF Defined	UI	Max	-		~~-~~	-		~~-~~	0.18 p-p (2.14 ps 1 sigma)		

Table 8 – OOB Specifications

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
V_{thresh}, OOB Signal Detection Threshold	mVppd	Min	50		~~120~~	75		~~120~~	75	Error! Reference source not found.	Error! Reference source not found.
		Nom	100		~~-~~	125		~~-~~	125		
		Max	200		~~240~~	200		~~240~~	200		
UI_{OOB},	ps	Min	646.67			646.67			646.67	Error!	-

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	**Gen1m**	**~~Gen1x~~**	**Gen2i**	**Gen2m**	**~~Gen2x~~**	Gen3i		
UI During OOB Signaling		Nom	666.67			666.67			666.67	**Reference source not found.**	
		Max	686.67			686.67			686.67		
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	ns	Min	103.5							**Error! Reference source not found. Error! Reference source not found.**	**Error! Reference source not found.**
		Nom	106.7								
		Max	109.9								
COMINIT/ COMRESET Transmit Gap Length	ns	Min	310.4							**Error! Reference source not found.**	**Error! Reference source not found.**
		Nom	320.0								
		Max	329.6								
COMWAKE Transmit Gap Length	ns	Min	103.5							**Error! Reference source not found.**	**Error! Reference source not found.**
		Nom	106.7								
		Max	109.9								

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	~~Gen1x~~	Gen2i	Gen2m	~~Gen2x~~	Gen3i		
COMWAKE Gap Detection Windows	ns	May detect	35 ≤ T < 175							**Error! Reference source not found.**	**Error! Reference source not found.**
		Shall detect	101.3 ≤ T ≤ 112								
		Shall not detect	T < 35 or T ≥175								
COMINIT/ COMRESET Gap Detection Windows	ns	May detect	175 ≤ T < 525							**Error! Reference source not found.**	**Error! Reference source not found.**
		Shall detect	304 ≤ T ≤ 336								
		Shall not detect	T < 175 or T ≥ 525								

7.2.2.1.7 DC Coupled Common Mode Voltage (Gen1i)

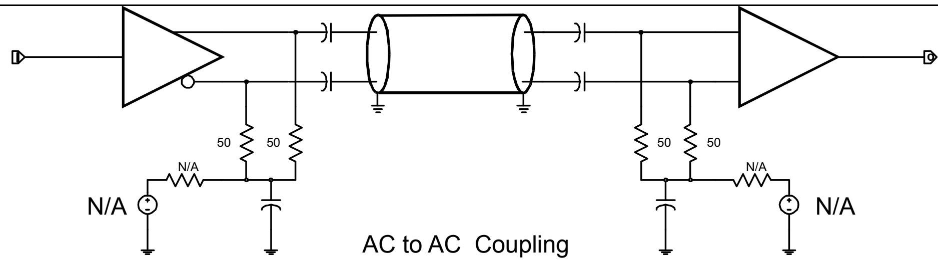
The Common mode DC level is defined as [(TX+) + (TX-)]/2 and [(RX+) + (RX-)]/2 measured at the mated connector.

This requirement only applies to Gen1i DC-coupled designs (no blocking capacitors) that hold the common-mode DC level at the connector. The four possible common mode biasing configurations shown in **Error! Reference source not found.** below demonstrate that only DC-coupled designs need sustain the specified common-mode level to ensure interoperability. AC coupled designs may allow the DC level at the connector to float. The SATA interfaces defined as ~~Gen1x,~~ Gen2i, ~~Gen2x,~~ and Gen3i shall be AC-coupled and this requirement does not apply to these.

7.2.2.1.8 AC Coupled Common Mode Voltage

The SATA interface, defined as Gen1i, may be AC or DC coupled as shown in **Error! Reference source not found.**. The SATA interfaces defined as ~~Gen1x,~~ Gen2i, ~~Gen2x,~~ and Gen3i shall be AC-coupled.
Figure 3 shows an example of a fully AC-coupled system.

Compliance points for SATA are defined at the connector. The AC coupled common mode voltage in Table 3 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled Phy and it shall be met during all possible power and electrical conditions of the Phy including power off and power ramping. Since the ~~Gen1x,~~ Gen2i, ~~Gen2x,~~ and Gen3i specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications. The common mode transient requirements defined in Table 3 were determined sufficient to limit stresses on the attached components under transient conditions, which was the sole intent of the AC, coupled common mode voltage requirement. Due to this, the following is true even for Gen1i where $V_{cm,ac\ coupled}$ applies: AC coupled common mode voltage levels outside the specified range may be used provided that the transient voltage requirements of Table 3 are met.



NOTE: For N/A, see Error! Reference source not found. **and** Error! Reference source not found.**.**

Figure 3 – Common Mode Biasing for ~~Gen1x,~~ Gen2i, ~~Gen2x,~~ and Gen3i

7.2.2.1.10 AC Coupling Capacitance

The value of the coupling capacitor used in AC coupled implementations. AC coupling is optional for Gen1i and mandatory of ~~Gen1x,~~ Gen2i, ~~Gen2x,~~ and Gen3i.

Coupling Capacitor Characteristics (Informative): The physical size of the capacitor should be as small as practical to reduce the capacitance to ground. Body sizes larger than 0603 (or values less than 300 pF) should be avoided since they are likely to result in a failure of the return loss requirements in **Error! Reference source not found.**, and **Error! Reference source not found.**.

The physical size of the capacitor should be as small as practical to reduce the capacitance to ground. Body sizes larger than 0603 should be avoided, as they are likely to result in a failure of the return loss requirements in Table 4 and Table 5.

7.2.2.2.11 TX AC Common Mode Voltage (Gen2i~~, Gen1x, Gen2x~~)

Maximum sinusoidal amplitude of common mode signal measured at the transmitter connector.

The Transmitter shall comply to the electrical specifications of section **Error! Reference source not found.**, when subjected to a sinusoidal interfering signal with peak-to-peak voltage, and swept from the frequency range extremes, at a sweep rate period no shorter than 33.33 us.

7.2.2.2.14 OOB Differential Delta (Gen2i,Gen3i, Gen2m~~,Gen1x, Gen2x~~)

The difference between the average differential value during the idle bus condition and the average differential value during burst on transitions to and from the idle bus condition.

During OOB transmission, imperfections and asymmetries in transmitters may generate error signals that impair proper detection by a receiver. The OOB Differential Delta describes an error from the difference in transmitter DC offset during the idle and active conditions. Since the transmitter is alternating between idle and active conditions each with different DC offsets, an AC error voltage is generated which is a square wave at about 1 / (2*106 ns) = 4.7 MHz. The AC error voltage propagates through the interconnect and causes an offset in the receiver OOB detector.

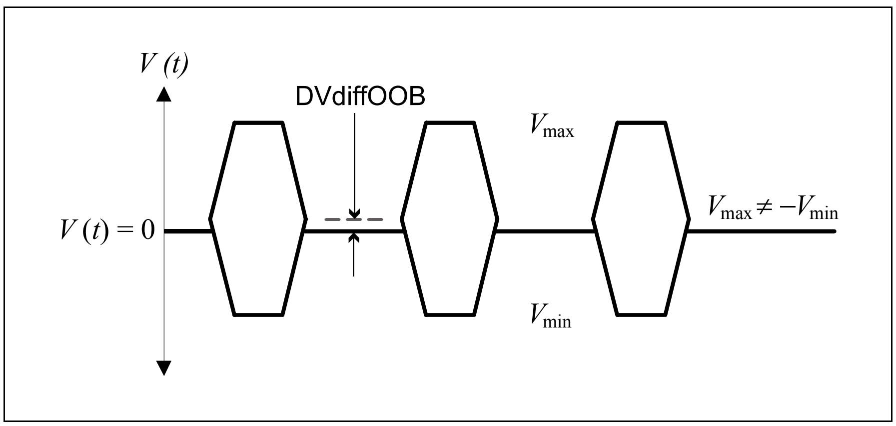


Figure 4 – OOB Differential Delta (at Compliance Point with AC Coupling)

7.2.2.2.15 OOB Common Mode Delta (Gen2i, Gen3i~~,Gen1x, Gen2x~~)

The difference between the common mode value during the idle bus condition and the common mode value during a burst on transitions to and from the idle bus condition.

7.2.2.2.17 TX Amplitude Imbalance (Gen2i~~, Gen1x, Gen2x~~)

The match in the amplitudes of TX+ and TX- determined by the function: absolute value (TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2 and all amplitudes are determined by mode (most prevalent) voltage.

7.2.2.2.18 Clock-to-Data Transmit Jitter (Gen1i, Gen1m, ~~Gen1x,~~ Gen2i, Gen2m, ~~Gen2x,~~ Gen3i)

Transmitters shall meet the jitter specifications for the Reference Clock characteristics specified in each case.

Table 5 shows the maximum amount of jitter that a transmitter may generate and still be SATA compliant and section 0 describes the measurement. Since this specification places the compliance point afterthe connector, any jitter generated at the package connection, on the printed circuit board, and at the board connector shall be included in the measurement.

7.2.2.5.4 RX Differential Skew (Gen2i, ~~Gen1x, Gen2x,~~ Gen3i)

RX Differential Skew is the time difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX- signal falling/rising edge, as measured at the RX connector. The receiver should tolerate the RX skew levels per Table 7, as generated by a Lab-Sourced Signal.

7.2.2.5.5 RX AC Common Mode Voltage (Gen2i~~, Gen1x, Gen2x~~)

Max peak-to-peak sinusoidal amplitude of AC common mode signal [(RX+) + (RX-)]/2.

The Receiver shall operate to within the frame error rate cited in Table 3, when subjected to a sinusoidal common mode interfering signal with peak-to-peak voltage $V_{cmRX,ac}$ defined in Table 7 and swept across the frequency range, $f_{cm,acRX}$, defined in Table 7 at a sweep rate period no shorter than 33.33 us.

7.2.2.5.7 Clock-Data Receiver Jitter Tolerance (Gen1i, Gen1m, Gen2i, Gen2m, ~~Gen1x, Gen2x~~)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 7 and section 0 describes the measurement for Gen1 and Gen2.

7.2.5 Hot Plug Considerations

7.2.5.1 Hot Plug Overview

The purpose of this section is to provide the minimum set of normative requirements necessary for a Serial ATA Host or Device to be declared as "Hot-Plug Capable". As there exists various Hot-Plug events, there are relevant electrical and operational limitations for each of those types of events. The events are defined below, and the Hot-Plug Capability is further classified into:

a) Surprise Hot-Plug capable
b) OS-Aware Hot-Plug capable

When a Host or Device is declared Hot-Plug Capable without any qualifier, this shall imply that the SATA interface is Surprise Hot-Plug Capable.

For the purposes of this specification, Hot-Plug operations are defined as insertion or removal operations, between SATA hosts and devices, when either side of the interface is powered.

~~Gen1x / Gen 2x /~~ Gen1m and Gen2m interfaces shall meet the requirements to be classified as Hot-Plug Capable. These requirements are not applicable to Gen1i and Gen2i cabled interfaces, however, Gen1i/Gen2i Devices used in Short Backplane applications shall be Hot-Plug Capable.

Hot-Plug Capable Hosts/Devices shall not suffer any electrical damage, or permanent electrical degradation, and shall resume compliant Tx/Rx operations after the applicable OOB operations, following the Hot-Plug Events.

- **Asynchronous Signal Hot Plug / Removal:** A signal cable is plugged / unplugged at any time. Power to the Host/Device remains on since it is sourced through an alternate mechanism, which is not associated with the signal cable. This applies to External Single-Lane and Multilane Cabled applications.
- **Unpowered OS-Aware Hot Plug / Removal:** This is defined as the insertion / removal of a Device into / from a backplane connector (combined signal and power) that has power shutdown. Prior to removal, the Host is placed into a quiescent state (not defined here) and power is removed from the backplane connector to the Device. After insertion, the backplane is powered; both the Device and Host initialize and then operate normally. The mechanism for powering the backplane on/off and transitioning the Host into/out of the "quiescent" state is not defined here. During OS-Aware events, the Host is powered. This applies to "Short" and "Long" Backplane applications.
- **Powered OS-Aware Hot Plug / Removal:** This is defined as the removal of a Device into / from a backplane connector (combined signal and power) that has power on. After insertion, both the Device and Host initialize and then operate normally. Prior to insertion or removal, the Host is placed into a quiescent state (not defined here) but the backplane connector to the Device is powered at all times. The mechanism for transitioning the Host into/out of the "quiescent" state is not defined here. During OS-Aware events, the Host is powered. This applies to "Short" and "Long" Backplane applications.
- **Surprise Hot-Plug / Removal:** This is defined as the insertion / removal of a Host or Device into / from a backplane connector (combined signal and power) that has power on. After insertion, both the Device and Host initialize and then operate normally. The powered Host or Device is not in a quiescent state.

NOTE: This does not imply transparent resumption of system-level operation since data may be lost, the device may have to be re-discovered and initialized, etc. Regardless of the above definitions, the removal of a device, which is still rotating, is not recommended and should be prevented by the system designer.

7.2.7 Compliance Interconnect Channels (~~Gen1x, Gen2x,~~ Gen3i)

Compliance Interconnect Channels are defined as a set of calibrated physical test circuits applied to the Transmitter mated connector, intended to be representative of the highest-loss interconnects.

The Compliance Interconnect Channel (CIC) is used to verify that the signal electrical characteristics at the Transmitter mated connector are sufficient to ensure compliance to the input electrical specifications for ~~Gen1x, Gen2x and~~ Gen3i receivers as delivered through worst-case media. The magnitude of this worst-case loss as a function of frequency is defined mathematically as a Transmitter Compliance Transfer Function (TCTF). ~~There is a Gen3i TCTF, Gen2x TCTF and a Gen1x TCTF.~~ Any linear, passive, differential two-port (e.g., a SATA cable) with loss greater than the TCTF at all frequencies and which meets the ISI loss constraint (defined below) is defined to be a CIC. (See also section **Error! Reference source not found.**.)

A combination of a zero-length test load (i.e., the Laboratory Load) plus the applicable CIC (~~Gen1x/Gen2x/~~Gen3i) is used for the specification of the host-controller or device transmitter characteristics.

A ~~Gen1x/Gen2x/~~Gen3i transmitter signal is specified by:

1. Meeting all parameters in Table 5[1] for ~~Gen1x, Gen2x or~~ Gen3i when transmitting into a Laboratory Load.
2. ~~Meeting Table 5 input swing (V_{diffTX}) and jitter (TJ after CIC and DJ after CIC) requirements for Gen1x or Gen2x when transmitting through the appropriate Gen1x or Gen2x CIC into a Laboratory Load while using the same transmitter settings (emphasis, amplitude, etc.) as in the first test.[2] (see sections 0 and 0)~~
3. Meeting Table 5 input swing (VdiffTx) and total jitter (TJ after CIC) requirements for Gen3i when transmitting through the appropriate Gen3i CIC into a Laboratory Load while using the same transmitter settings (emphasis, amplitude, etc.) as in the first test.[2]

The transmission magnitude response, |S21|, of the Gen3i TCTF satisfies the following two inequalities[3]:

$$| S_{21} | \leq -20 \log_{10} (e) \{[3.0 \times 10^{-6} (f^{0.5})] + [1.1 \times 10^{-10} (f)] \} \text{ dB}$$

for 50 MHz < f < 9.0 GHz, (f expressed in Hz),

$$| S_{21} | \text{ at 600 MHz} - | S_{21} | \text{ at 3000 MHz} > 2.7 \text{ dB}$$

---

[1] Note that the Transmitter Compliance Specifications are defined and measured into a Laboratory Load. Received signal attenuation or amplification due to actual receiver terminator tolerance as well as additional received signal ISI due to the actual receiver return loss may further degrade the actual receiver's input signal. Transmitter Compliance Specifications are expected to be only slightly tighter than Receiver Specifications.

[2] While not permitted in this specification, this second requirement can be approximated by *mathematically* processing through a TCTF the signal captured by the HBWS using only the Laboratory Load in the first requirement.

[3] Please note that "e" in the first expression is the base of the natural logarithms, approximately 2.71828. Hence, the first factor, 20 $\log_{10}$(e), evaluates to approximately 8.6859. This value is the conversion factor from nepers (defined as the natural logarithm of a power ratio) to decibels.

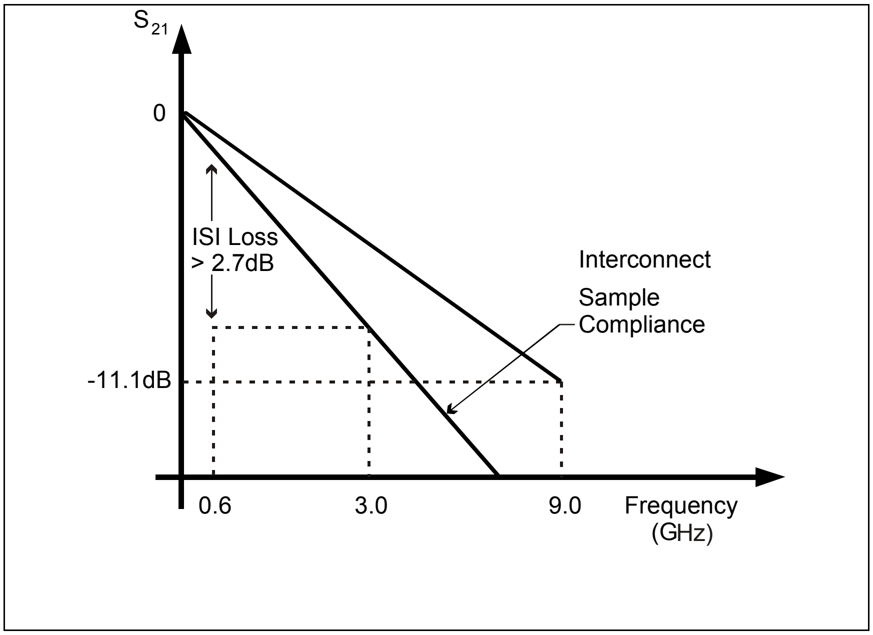


Figure 5 – Compliance Channel Loss for Gen3i

The second constraint, termed ISI loss, may be motivated as follows: $|S_{21}|$ at one tenth the data rate is the attenuation of the fundamental component of a repeating five-ones-five-zeroes pattern, the longest possible run lengths in 8b/10b encoded data. Similarly, $|S_{21}|$ at one half the data rate is the attenuation of the fundamental component of a repeating …010101… pattern, the shortest possible run lengths in 8b/10b encoded data. Hence, for an output waveform of this TCTF, ISI loss approximates the ratio between a) the peak-peak voltage (established by the long run lengths) and b) the inside vertical eye opening (established by the high frequency pattern). Any TCTF with a flatter loss characteristic (i.e., with more broadband attenuation) would generate less inter-symbol interference (ISI) and therefore less output jitter. This constraint prohibits such a TCTF.

~~The transmission magnitude response, $|S_{21}|$, of the Gen2x TCTF satisfies the following three inequalities[4]:~~

~~$| S_{21} | \leq -20 \log_{10}(e) \{[1.7 \times 10^{-5} (f^{0.5})] + [1.0 \times 10^{-10} (f)] \}$ dB~~

~~for 50 MHz < f < 3.0 GHz, (f expressed in Hz),~~

~~$| S_{21} | \leq -10.7$ dB~~

~~for 3.0 GHz < f < 5.0 GHz, and~~

~~$| S_{21} |$ at 300 MHz - $| S_{21} |$ at 1500 MHz > 3.9 dB~~

---

[4] ~~Please note that "e" in the first expression is the base of the natural logarithms, approximately 2.71828. Hence, the first factor, $20 \log_{10}(e)$, evaluates to approximately 8.6859. This value is the conversion factor from nepers (defined as the natural logarithm of a power ratio) to decibels.~~

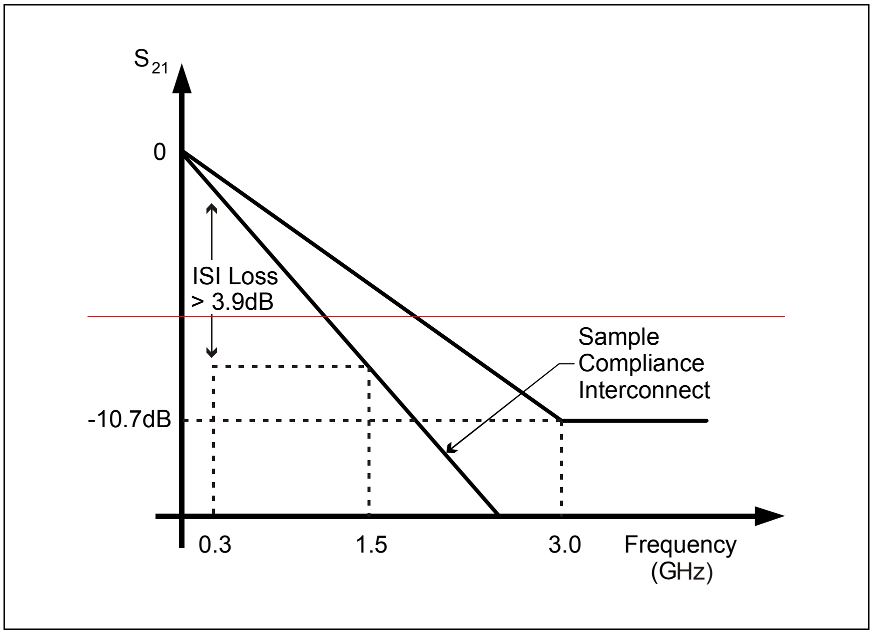


Figure 6 – Compliance Channel Loss for Gen2x

The third constraint, termed ISI loss, may be motivated as follows: $|S_{21}|$ at one tenth the data rate is the attenuation of the fundamental component of a repeating five-ones-five-zeroes pattern, the longest possible run lengths in 8b/10b encoded data. Similarly, $|S_{21}|$ at one half the data rate is the attenuation of the fundamental component of a repeating …010101… pattern, the shortest possible run lengths in 8b/10b encoded data. Hence, for an output waveform of this TCTF, ISI loss approximates the ratio between a) the peak-peak voltage (established by the long run lengths) and b) the inside vertical eye opening (established by the high frequency pattern). Any TCTF with a flatter loss characteristic (i.e., with more broadband attenuation) would generate less inter-symbol interference (ISI) and therefore less output jitter. This constraint prohibits such a TCTF.

The transmission magnitude response, $|S_{21}|$, of the Gen1x TCTF satisfies the following three inequalities:

$| S_{21} | \leq -20 \log_{10} (e) \{[1.7 \times 10^{-5} (f^{0.5})] + [1.0 \times 10^{-10} (f)] \}$ dB

for 50 MHz < f < 1.5 GHz, (f expressed in Hz),

$| S_{21} | \leq -7.0$ dB

for 1.5 GHz < f < 5.0 GHz, and

$| S_{21} |$ at 150 MHz - $| S_{21} |$ at 750 MHz > 2.0 dB

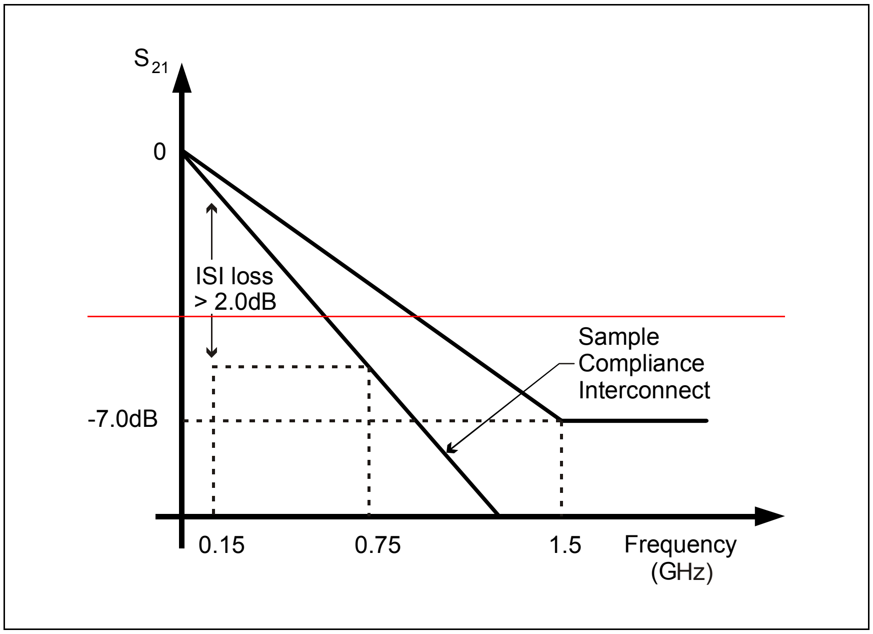


Figure 7 – Compliance Channel Loss for Gen1x

~~7.3.2.3 Gen1x and Gen2x Normative Requirements~~

~~For Gen1x and Gen2x, the Reference Clock PLL is defined as type 2 PLL with a -3 dB corner frequency $f_{c3dB} = f_{BAUD}$ /1667 given a transition density of 1.0 (corresponding to a 1010101010 clock-like pattern) and damping factor ξ = 0.707 min to 1.00 max.~~

7.4.5 Transmitter Amplitude

The transmitter amplitude values specified in Table 5 refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1m, Gen2m, ~~Gen1x, Gen2x,~~ and Gen3i), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for ~~Gen1x, Gen2x, and~~ Gen3i only). The signals are not specified when attached to a system cable or backplane.

7.4.8 Jitter Measurements

Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition. The causes of jitter are categorized into random sources (RJ) and deterministic sources (DJ). Although the total jitter (TJ) is the convolution of the probability density functions for all the independent jitter sources, this specification defines the random jitter as Gaussian and the total jitter as the deterministic jitter plus 14 times the random jitter. The TJ specifications of Table 5 and Table 7 were chosen at a targeted BER of 10^{-12}. The BERT scan method described in section **Error! Reference source not found.** is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. The method for estimating TJ is unique to each measurement instrument.

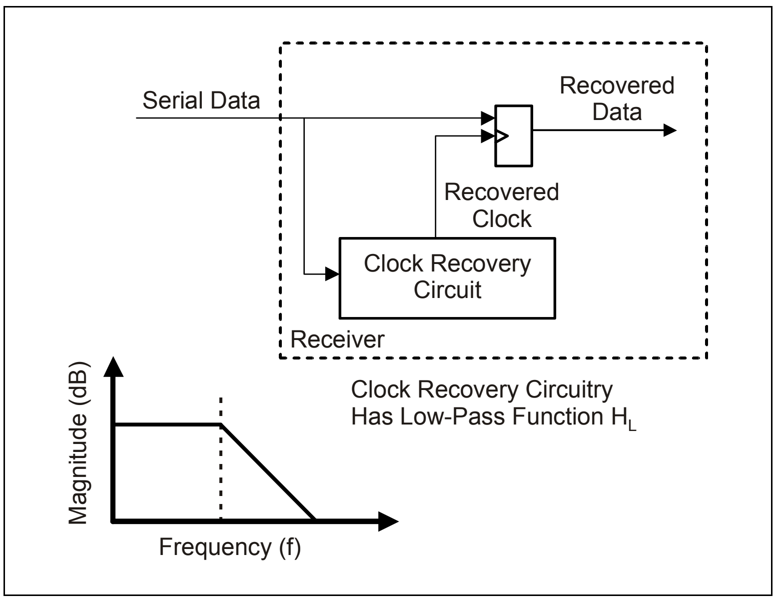


Figure 8- Receiver Model for Jitter

The jitter measurement methodology is defined as a clock to data jitter measurement. Figure 8 shows a block diagram of a deserializer input. The serial data is split into two paths. One path feeds clock recovery circuitry, which becomes the reference signal used to latch the data bits of the serial data stream. This clock recovery circuitry has a low pass transfer function H_L. This low pass function is the CLTF of the PLL or clock recovery circuit. The jitter seen by the receiver is the time difference of the recovered clock edge to the data edge position. This time difference function is shown in Figure 9. The resulting jitter seen by the receiver has a high pass function H_H shown in Figure 10. This high pass function is the JTF (Jitter Transfer Function) of the system. This defines the measurement function required by all jitter measurement methodologies. The required characteristics for the JTF (Gen1i, Gen1m, Gen2i, Gen2m) and the CLTF corner

frequency f_c ~~(Gen1x, Gen2x)~~ are provided in section 7.3.2. In the case of a JMD, the JTF may be simply viewed as the ratio of the reported jitter to the applied jitter, for a sinusoidal PJ input.
Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the rationale for Gen1i, Gen1m, Gen2i and Gen2m directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.

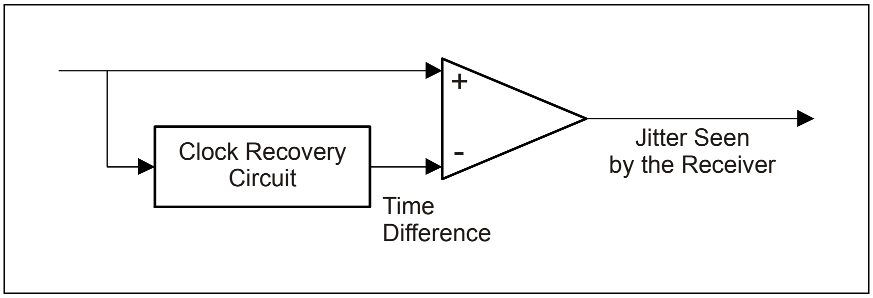


Figure 9 – Jitter at Receiver

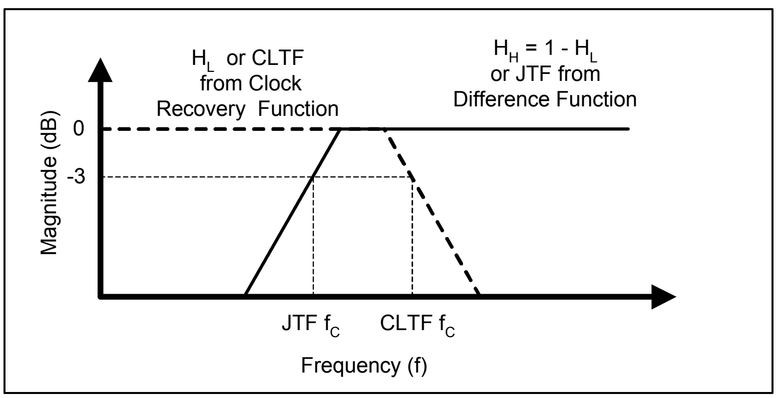


Figure 10 – Jitter at Receiver, High Pass Function

This JTF (H_H in Figure 10) mimics the receiver's ability to track lower frequency jitter components (wander, SSC) and not include them in the jitter measurement. This measurement methodology enables any measurement instrument to accurately measure the jitter seen by a receiver and produce measurements that correlate from measurement instrument to measurement instrument.

It should be noted that the corner frequency of the JTF is not the corner frequency of the clock recovery CLTF. This may not be obvious until one considers the phase shift caused by the clock recovery circuit. In general the vector sum $H_L(f) + H_H(f) = 1$. All quantities consist of changing magnitude and phase as a function of frequency. This accounts for differences in corner frequencies and peaking in the two frequency dependant functions.

Figure 11 shows more detail into how the JTF and CLTF relate to the jitter that would be applied to a receiver. The subfigure A) represents a generic control system block diagram for a feedback loop based clock recovery system. Subfigure B) translates the same complex variables to the combined system of the clock recovery circuit and the time difference function. It can be seen that E(s) is the jitter seen by the receiver, as well as being the error signal in the clock recovery circuit. Subfigure C) provides the defining equations for the clock recovery circuit CLTF and the combined system JTF function.

Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the rational for Gen2i, Gen2m, and Gen3i: directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.

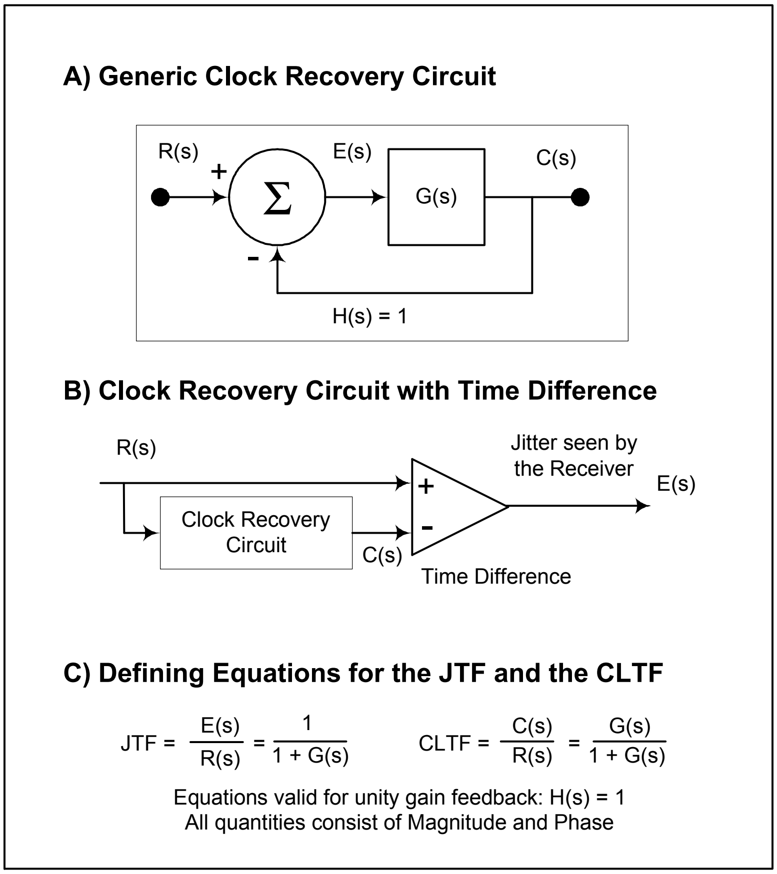


Figure 11 – JTF and CLTF Definition

7.4.9 Transmit Jitter (Gen1i, Gen2i, Gen1m, Gen2m~~, Gen1x, and Gen2x~~)

The transmit jitter values specified in Table 5 refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1m, Gen2m, ~~Gen1x, and Gen2x), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen1x and Gen2x~~). The signals are not specified when attached to a system cable or backplane. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter.

Transmit jitter is measured with each of the specified patterns in section **Error! Reference source not found.**. The measurement of jitter is described in section 0. Transmit jitter is measured in one of the following two setups ~~for Gen2i and both setups for Gen1x and Gen2x~~. ~~For Gen1i, Gen2i, Gen1x, and Gen2x~~ the transmitter is connected directly into the Laboratory Load (LL) shown in Figure 12. ~~Additionally, for Gen1x and Gen2x the transmitter is connected through the Compliance Interconnect Channel (see section 0) into the Laboratory Load shown in Figure 13.~~

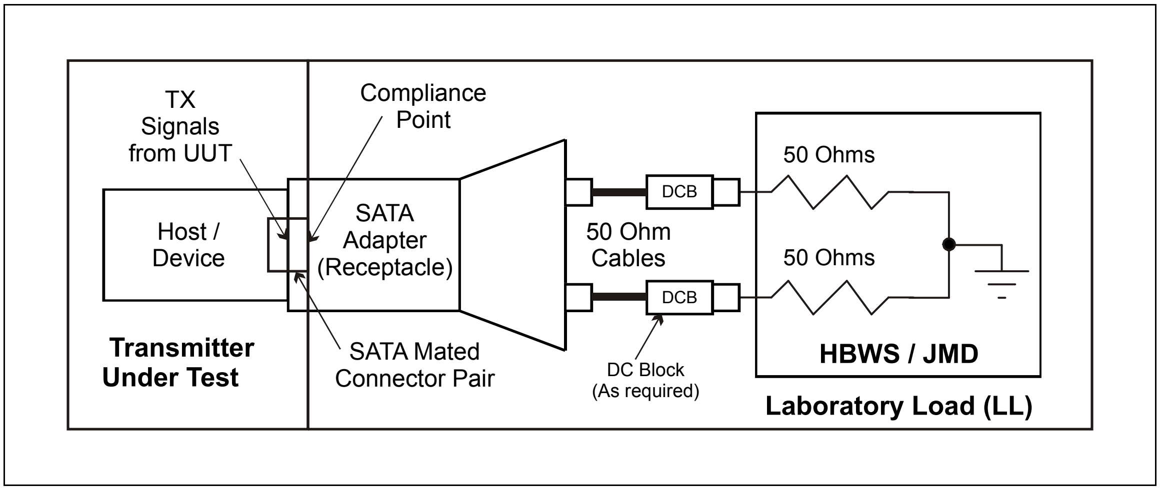
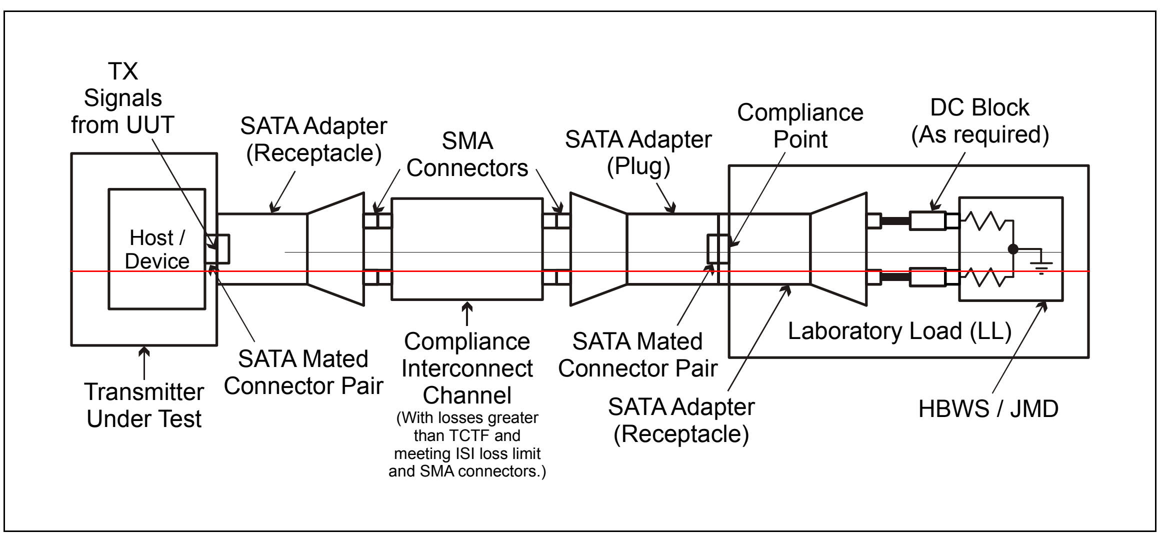


Figure 12 – Transmitter Jitter Test (Gen1i, Gen2i)



~~Figure 13 – Transmit Jitter Test with Compliance Interconnect Channel (Gen1x, Gen2x)~~

Transmitter jitter is measured into the Laboratory Load (LL), or in conjunction with the Compliance Interconnect Channel; both have very good impedance matching. The jitter in an actual system is higher since load and interconnect mismatch results in reflections and additional data dependent jitter. It is generally not possible to remove the effects of the SATA adapter on jitter since jitter due to mismatch depends on the entire test setup.

7.4.11 Receiver Tolerance (Gen1i, Gen2i, Gen1m, Gen2m~~, Gen1x, and Gen2x~~)

The performance measure for receiver tolerance and common mode interference rejection is the correct detection of data by the receiver. When measuring receiver and Common Mode tolerance it is necessary to set the maximum allowable jitter and common mode interference on the signal sent to the receiver and monitor data errors.