SyntheSys Research, Inc.

Serial ATA International Organization

Revision 1.0
June 7, 2006

Serial ATA Interoperability Program

Method of Implementation (MOI) for PHY and TSG Device Certification Tests

using the BERTScope by SyntheSys Research, Inc.

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MODIFICATION RECORD

First draft, January 25, 2006

Version 0.8, February 6, 2006

Version 0.93RC, March 14, 2006

Version 0.94RC, March 22, 2006: “using either the BIST T,S,A mode or other suitable method” inserted in the initiating step in PHY-01 through TSG-12. TSG01 section inserted. “Possible Issues” inserted in TSG-02. TSG04 removed one cable to improve the setup and corrected labels in step 4. TSG05 and TSG06 corrected to: “at least 10,000 samples” and “mean” Amplitude Imbalance. Inserted: “When initiating via BIST; there is 50% “in Possible Issues in TSG-09 through TSG-12. “This test requirement is only applicable to components claiming to be capable of running at 3Gb/s” inserted in TSG-11 and TSG-12. Appendix C step-by-step bullets filled in.

Version 0.96RC, March 23, 2006: Completed step 4 through 9 and observable results paragraphs of TSG01 and added “When calibrating the BERTScope clock need to be used. By clicking on “Synthesizer” the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the “Outputs On/Off” button. “to TSG-02.

Version 0.97RC, April 19, 2006: “SATAI (3.0)” corrected to “SATAI (6.0) in PHY-01 through TSG-02 and in TSG-09 and TSG-10. TSG-01 changed to minimum and maximum measured using the same method and TSG-02 merely using HFTP as described in Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc.

Version 0.98RC, June 1, 2006: Changed from “(6.0)” to “(1.98)” settings on the CR 12500A in PHY-01 through PHY-04. Updated TSG-01 and Appendix E. Updated PHY-01, PHY-04 and TSG-01 through TSG-03 with explicit requirements to save calibration screen shots. Updated TSG-09 and TSG-10 with TIE based methodology requirements of Unified Test Document, LogoTF_ILunified_v1_0RC2i.doc.

Version 0.99RC, June 7, 2006: Updated index to show TSG-01. Added reference to Comax H303000204 or equivalent in all sections. Detailed the scope measurements in PHY-03 and PHY-04.

Version 1.0RC, June 19, 2006: Modified SSC equations in PHY-04 to record SSC relative to $f_{nominal}$.

INTRODUCTION

These Methods of Implementations describe the step by step procedures to perform the required PHY-01 through PHY-04 and TSG-01 through TSG-12 (except TSG-07 and TSG-08, which are optional for all components) tests of the Serial ATA Interoperability Program using the BERTScope by SyntheSys Research, Inc. in order to qualify a device for listing on the SATA Integrators List.

The test setup is illustrated in Appendix B.

The tests may be performed in the sequence shown in Appendix E or automated using software. Please contact SyntheSys Research, Inc. at +1 (650) 364-1853 or info@bertscope.com for the availability of such software.

REFERENCES

The following document is referenced in this text:

[1] Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf
[2] Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2i.doc
[3] Serial ATA Interoperability Program Policy Document, LogoTF_Policy_v1_0RC2c.doc

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Test Title: PHY-01 : Unit Interval

Purpose: Verify that the Device Under Test, DUT, meets the Unit Interval specification of section 7.2.2.1.3 of Serial ATA revision 2.5 at both 1.5 Gb/s and 3 Gb/s if the DUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

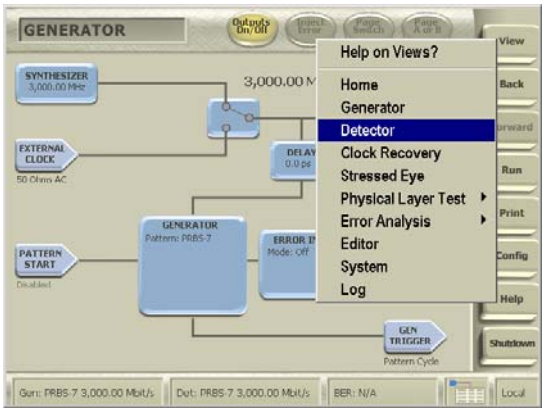
Last Modification: June 1, 2006

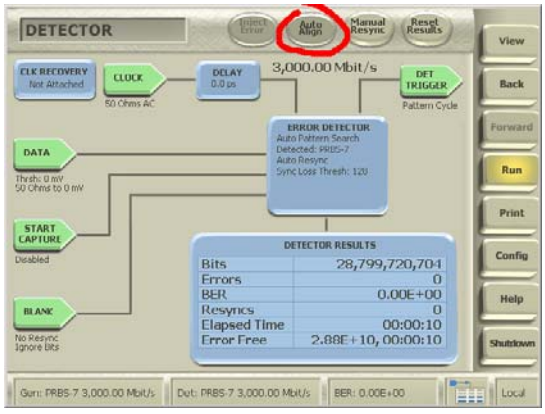
Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope automatically perform the Unit Interval measurement according to section 7.2.2.1.3 of the Serial ATA revision 2.5 based on more than 100,000 UIs.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

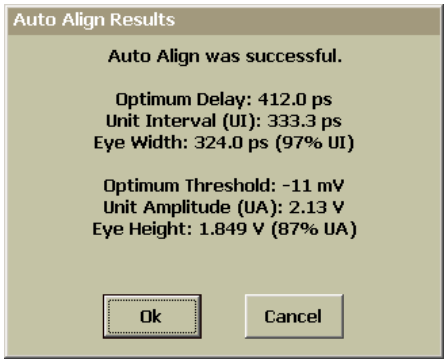
Test Procedure:

1. Initiate the DUT in transmitting the HFTP pattern (D10.2) using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the DUT to the iSATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
4. On the BERTScope, Select "View" then "Detector" and click on "Auto Align".





A pop-up window will appear with the Unit Interval measurement result.



5. Record the measured Unit Interval.
6. If the DUT claim to be capable of running at 3 Gb/s then repeat 1 through 5 of above to get both 1.5 Gb/s and 3 Gb/s measurements.

Observable Results: The pass/fail criteria are:

- Mean Unit Interval measured shall be between 666.4333ps (min) and 670.2333ps (max) (for components when running at 1.5Gb/s)
- Mean Unit Interval measured shall be between 333.2167ps (min) and 335.1167ps (max) (for components claiming to be capable of running at 3Gb/s)

Test Title: PHY-02 : Frequency Long Term Stability

Purpose: Verify that the Device Under Test, DUT, meets the Frequency Long Term Stability specification of section 7.2.2.1.4 of Serial ATA revision 2.5.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

Last Modification: June 1, 2006

Discussion: This test is only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). The BERTScope CR12500A has a built-in frequency counter that automatically performs the frequency measurement according to section 7.4.6 of the Serial ATA revision 2.5. If support of SSC is claimed by the device, the reported result must be the maximum value from the range of SSC modulation deviation, which is obtained by using the following formula: $f_{tol} = (f_{measured} - f_{nominal})/f_{nominal} + SSC_{deviation\_measured}/2f_{nominal}$. $f_{nominal}$ is 1.5 GHz for DUTs running at 1.5 Gb/s and 3 GHz for DUTs claiming to be capable of running at 3 Gb/s.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. Initiate the DUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the DUT claims to capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the DUT to the iSATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing Enter, scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
4. Record the measured frequency from the CR 12500A display.
5. Convert the measured frequency to ppm using the following formula: $f_{tol} = (f_{measured} - f_{nominal})/f_{nominal} + SSC_{deviation\_measured}/2f_{nominal}$, where SSC_{tol} is the spread-spectrum modulation deviation measured in PHY-04. $SSC_{deviation\_measured}$ is 0 if the DUT is not claimed to be SSC capable; $f_{nominal}$ is 1.5 GHz for DUTs running at 1.5 Gb/s and 3 GHz for DUTs claiming to be capable of running at 3 Gb/s. Record this value as the measured Frequency Long Term Stability.

Observable Results: The pass/fail criterion is:

- f_{tol} shall be between -350 ppm and 350 ppm.

Test Title: PHY-03 : Spread-Spectrum Modulation Frequency

Purpose: Verify that the Device Under Test, DUT, meets the Spread-Spectrum Modulation Frequency specification of section 7.2.2.1.5 and 7.3.3 of Serial ATA revision 2.5.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One Oscilloscope, Tektronix TDS3064B or equivalent having a bandwidth greater than 1 MHz.

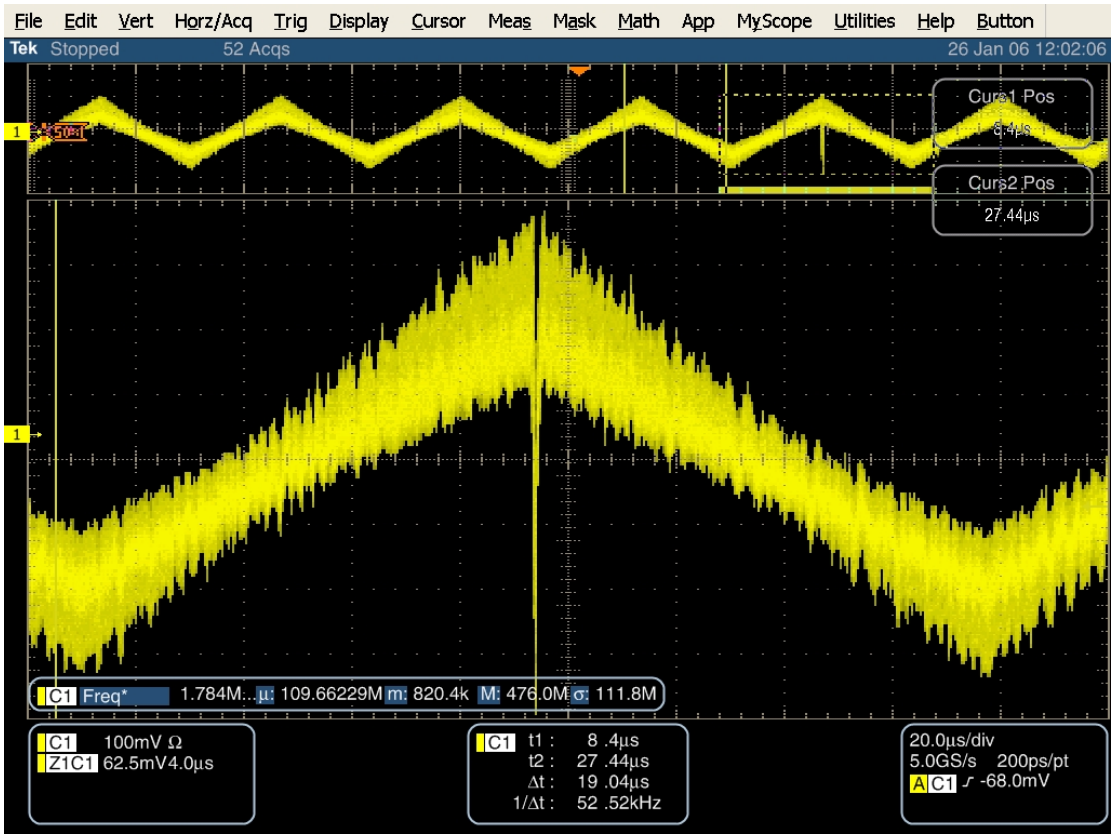
Last Modification: June 1, 2006

Discussion: This test is only run on a DUT claiming SSC operation and only run at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). The BERTScope CR 12500A automatically demodulate the incoming data signal and provides a signal on the rear panel output that represent the frequency deviation of the incoming data signal. The oscilloscope displays the spread-spectrum modulation waveform and measures the Spread-Spectrum Modulation Frequency according to section 7.4.11 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports. **Additional Connection:** Connect the CR 12500A rear panel output marked Frequency Tracking to the input port on the Oscilloscope.

Test Procedure:

1. Initiate the DUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the DUT claims to be capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the DUT to the iSATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
4. On the Oscilloscope, measure the average repetition frequency of the triangular waveform over at least 10 cycles of the SSC waveform.



5. Record the measured Spread-Spectrum Modulation Frequency.

Observable Results: The pass/fail criterion is:

- The measured Spread-Spectrum Modulation Frequency, f_{SSC}, shall be between 30 kHz and 33 kHz.

Test Title: PHY-04 : Spread-Spectrum Modulation Deviation

Purpose: Verify that the Device Under Test, DUT, meets the Spread-Spectrum Modulation Deviation specification of section 7.2.2.1.6 and 7.3.3 of Serial ATA revision 2.5.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One Oscilloscope, Tektronix TDS3064B or equivalent having a bandwidth greater than 1 MHz.

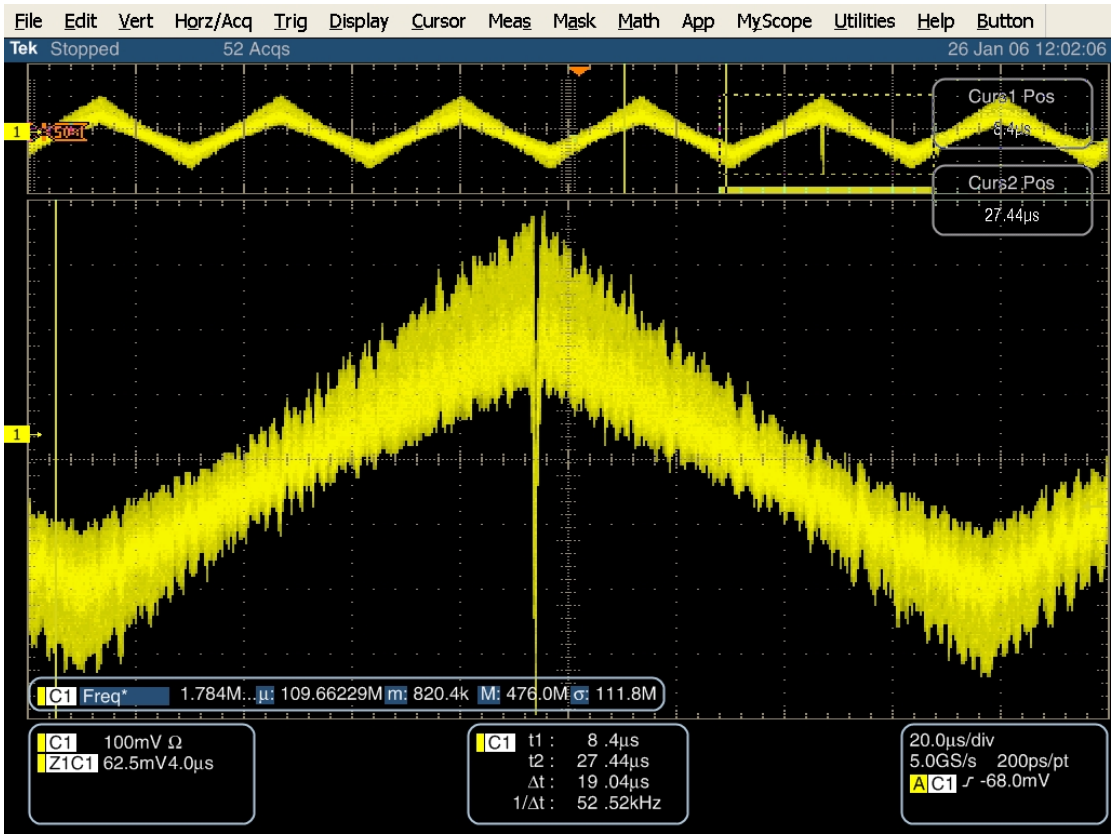
Last Modification: June 1, 2006

Discussion: This test is only run on a DUT claiming SSC operation and only run at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). The BERTScope CR 12500A automatically demodulate the incoming data signal and provides a rear panel output with a voltage proportional to the frequency deviation of the incoming data signal. The oscilloscope displays the spread-spectrum modulation waveform and measures the Spread-Spectrum Modulation Frequency. The value reported as the result is the single total range value (i.e. nominal to min) of the SSC modulation deviation according to section 7.4.11 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports. **Additional Connection:** Connect the CR 12500A rear panel output marked Frequency Tracking to the input port on the Oscilloscope.

Test Procedure:

1. Initiate the DUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the DUT claims to be capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the DUT to the iSATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: "SATAI (1.98)" for 1.5 Gb/s or "SATAII (1.98)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
4. On the Oscilloscope, measure the average of peak-to-peak amplitude over at least 10 of the SSC waveforms (commonly triangular or Lexmark shape). This is the spread-spectrum-modulation deviation expressed in voltage.



5. Record the measured spread-spectrum modulation deviation voltage from the Oscilloscope. Convert the spread-spectrum modulation deviation voltage to spread-spectrum modulation deviation frequency, $SSC_{deviation\_measured}$, by multiplying the recorded spread-spectrum deviation voltage by the frequency-versus-voltage sensitivity of the Frequency Tracking output from the calibration data, see Appendix C for frequency-versus-voltage calibration of the Frequency Tracking output.
6. Convert the measured spread-spectrum modulation deviation voltage to Spread-Spectrum Modulation Deviation in ppm relative to $f_{nominal}$ using the following formula: $SSC_{tol} = (f_{measured} - f_{nominal})/f_{nominal} - SSC_{deviation\_measured}/2f_{nominal}$, where $f_{nominal}$ is 1.5 GHz for DUTs running at 1.5 Gb/s and 3 GHz for DUTs claiming to be capable of running at 3 Gb/s and record this value as the measured Spread-Spectrum Modulation Deviation.

Observable Results: The pass/fail criterion is:

- The measured Spread-Spectrum Modulation Deviation, SSC_{tol}, shall be between -5000 ppm and +0 ppm.

Test Title: TSG-01 : Differential Output Voltage

Purpose: Verify that the Device Under Test, DUT, meets the Differential Output Voltage specification of section 7.2.2.3.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP, LFTP and LBP at both 1.5 Gb/s and 3 Gb/s if the DUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

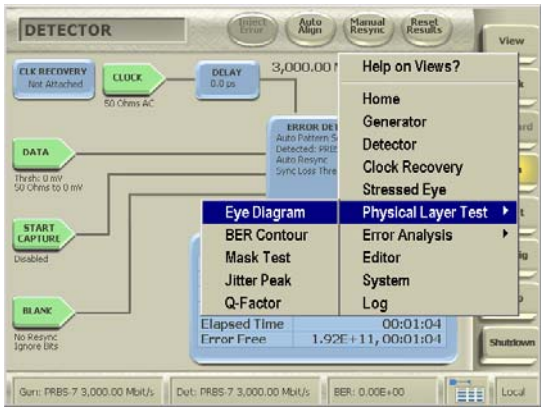
Last Modification: June 1, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope simultaneously captures the amplitudes for various bits in described set-up according to section 7.4.2 of the Serial ATA revision 2.5.

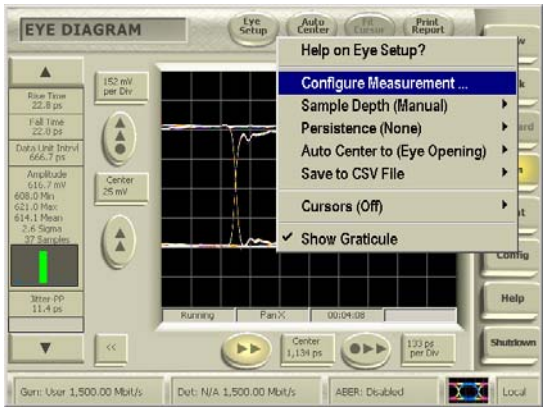
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

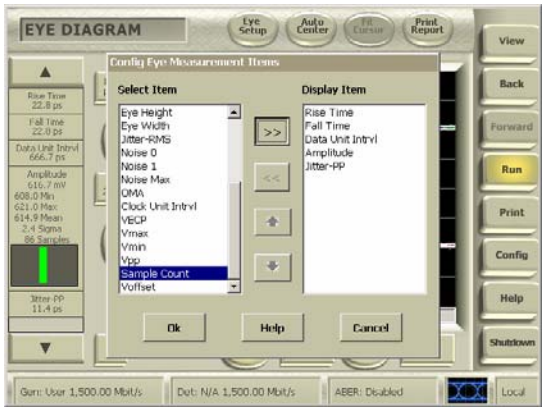
Test Procedure:

1. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (6.0)" for 1.5 Gb/s or "SATA2 (6.0)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the DUT transmitting the HFTP pattern using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center".

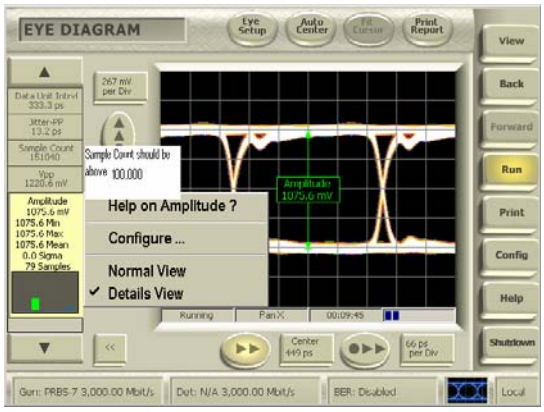


Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Check that the sample size is set for 10,000 or higher by clicking on "Eye Setup" then "Configure Measurement…" select "Sample Count" and click on ">>" and "OK".





5. Click on the "Amplitude" measurement field on the left side bar and select "Detailed View".

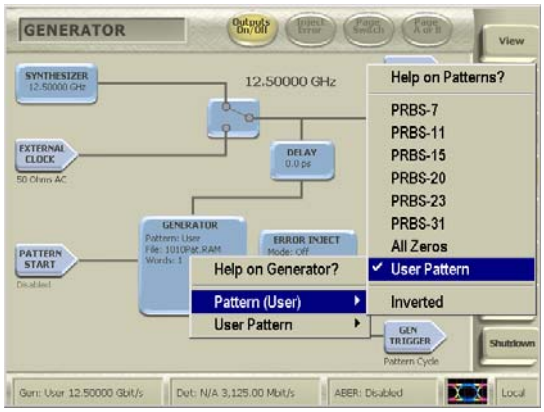


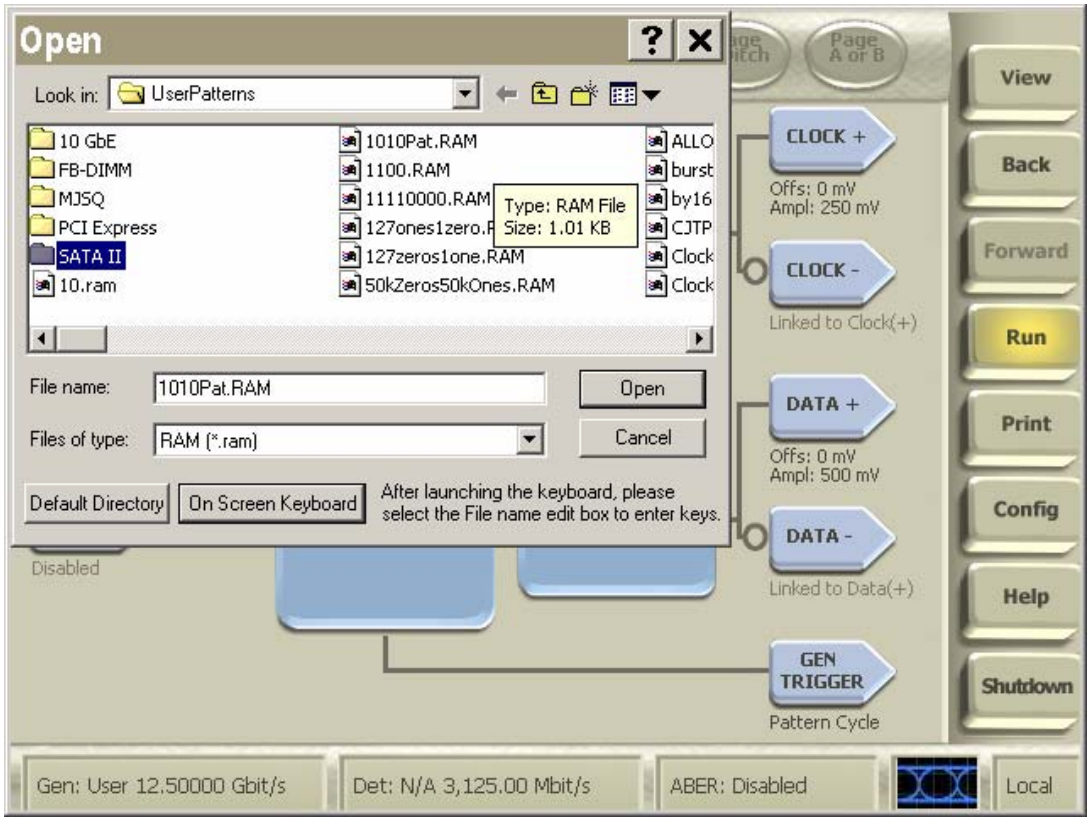
Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value DH = [x – (1.96 s /√ n)].

6. On the CR12500A scroll down to "SubDiv: 1", press "Enter" and scroll to select "2" and click "Enter
7. Repeat 2 through 4 with the DUT initiated transmitting the MFTP pattern and using the cursor to measure the amplitude at the second "1" and "0" which is 0.5 UI from the center of the MFTP "1100" eye. Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value DM = [x – (1.96 s /√ n)].
8. On the CR12500A scroll down to "SubDiv; 2", press "Enter" and scroll to select "10" and click "Enter".
9. Repeat 2 through 4 with the DUT initiated transmitting the LBP pattern this time measuring the amplitude of the lone bit.. Verify that the right disparity of the LBP is received by selecting "View" then "Editor" on the BERTScope. Click "File" then "Capture By Length". Click "OK" to override RAM. Enter "5" words and click "OK". Toggle the view to binary by click on "Edit" then "Display Format" and "Binary".

Verify that the pattern contains the "00001000" sequence on which the amplitude is to be measured on the lone "1" bit . Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value VTestLBP = $[x - (1.96\ s / \sqrt{n})]$.

10. Record the smallest value of DM and VTestLBP as the minimum differential voltage, VdiffTX(Min) and the largest value of DM and VTestLBP as the maximum voltage, VdiffTX(Max).
11. If the DUT claims to be capable of running at 3 Gb/s then repeat 1 through 10 of above to get both 1.5 Gb/s and 3 Gb/s measurements.
12. Calibrate the test set up by repeating 1 through 11 above using the same patterns, but generated by the pattern generator of the BERTScope connected via the short matched pair of cables first in place of the iSATA receptacle to SMA Female Adapter and the DUT and then compare these measured values to a set measured with the BERTScope Data Output ports directly to the Data Input ports of the BERTScope. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. The ratio of amplitude measured through the CR 12500A and cables compared to the amplitude measured directly is the amplitude calibration factor,, which accounts for the cable and CR 12500A insertion loss. The patterns are pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern.





When calibrating; the BERTScope clock need to be used. By clicking on "Synthesizer" the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the "Outputs On/Off" button. The calibrated measurement values are the amplitudes measured from the DUT divided by the amplitude calibration factors.

Observable Results: The pass/fail criteria are:

- The measured minimum differential voltages, VdiffTX(Min), shall both be larger than 400 mV (at 1.5 Gb/s as well as at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s)
- Each of the measured maximum differential voltages, VdiffTX(Max), shall be less than 800 mV (at 1.5 Gb/s as well as at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s)

Test Title: TSG-02 : Rise/Fall Time

Purpose: Verify that the Device Under Test, DUT, meets the Rise and Fall Time specification of section 7.2.2.3.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) at both 1.5 Gb/s and 3 Gb/s if the DUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

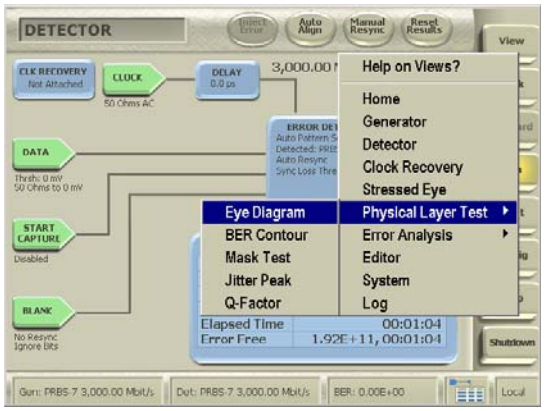
Last Modification: June 1, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope simultaneously measures the 20% to 80% Rise and 80% to 20% Fall times by default according to section 7.4.3 of the Serial ATA revision 2.5.

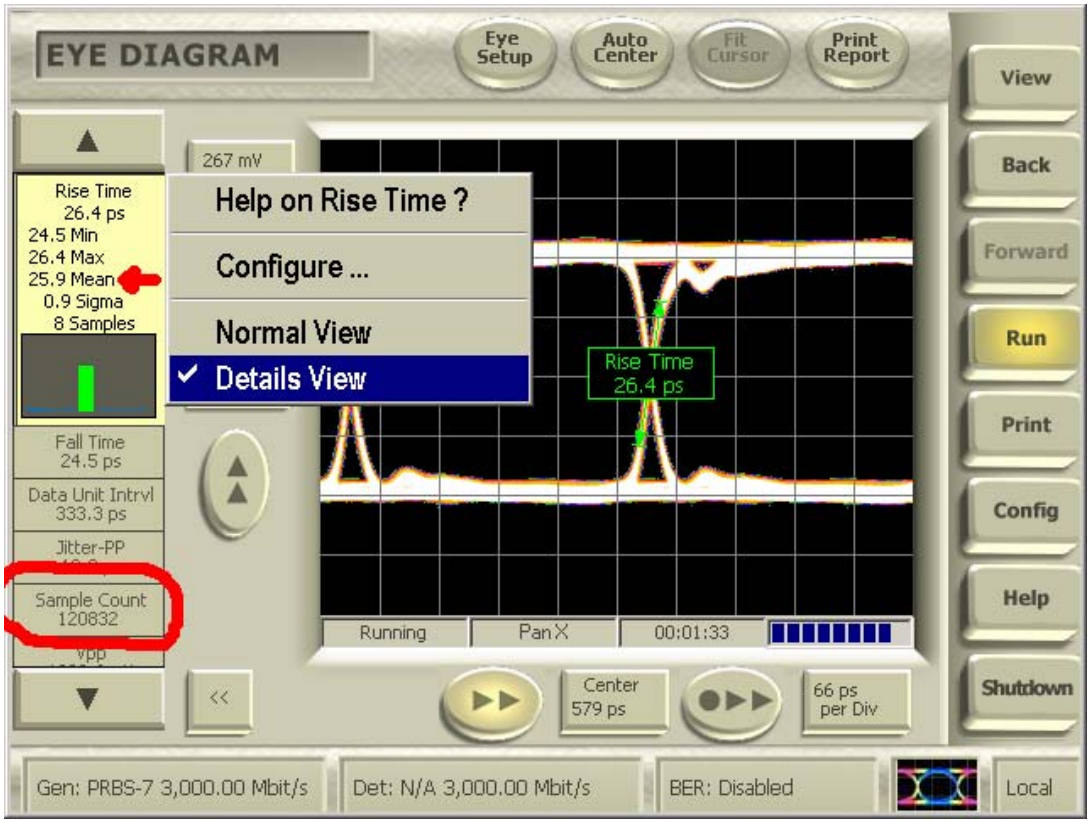
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

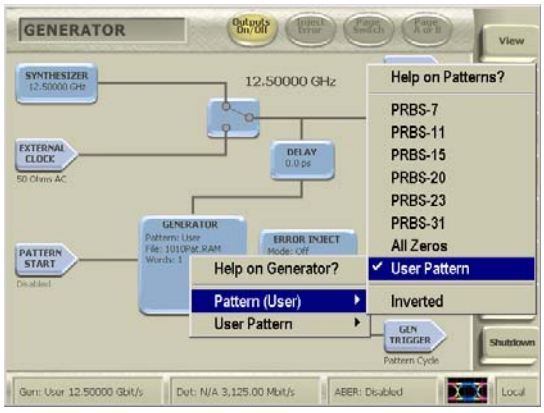
1. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (6.0)" for 1.5 Gb/s or "SATA2 (6.0)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the DUT transmitting the HFTP pattern (D10.2) using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center".

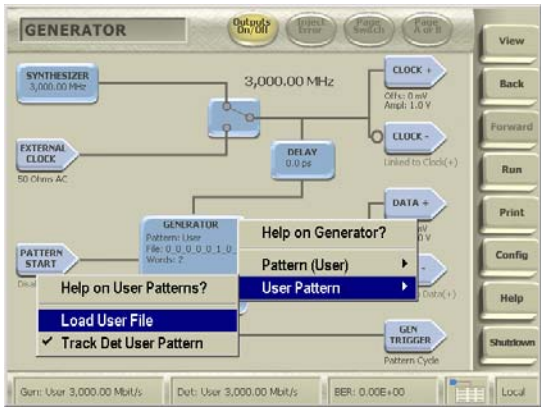


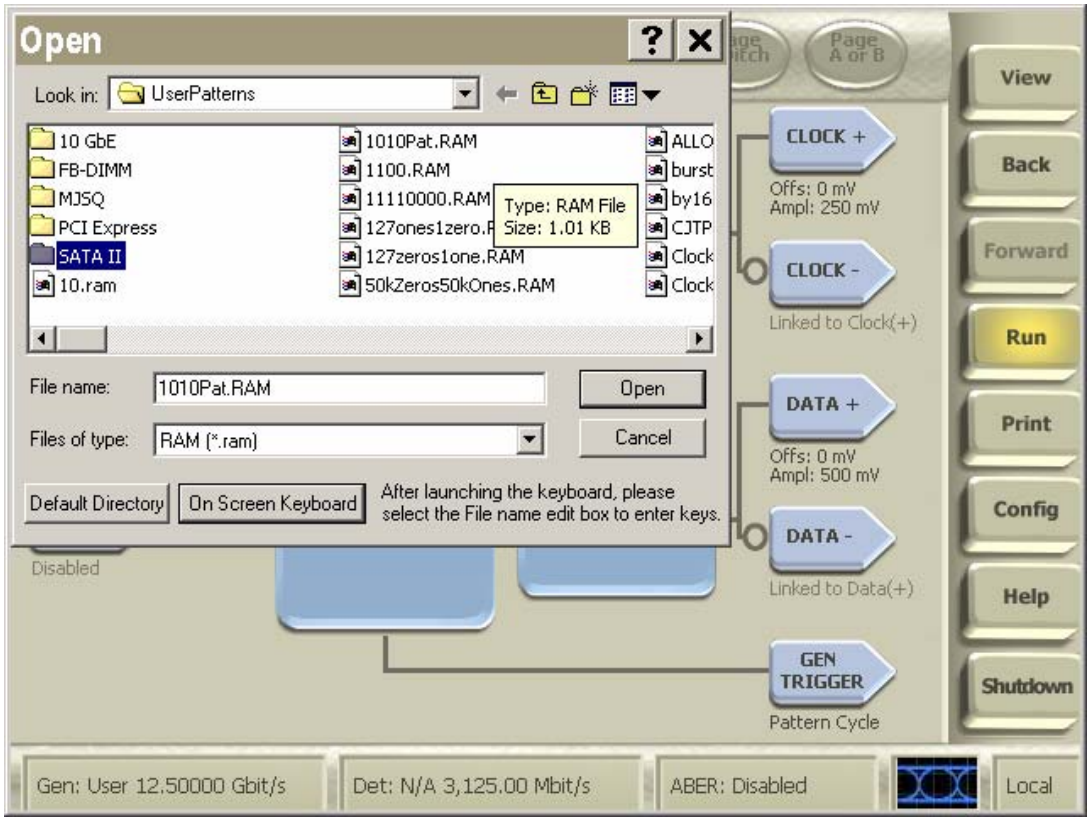
Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Click on the "Rise Time" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reach 100,000 and record the mean Rise Time value.



5. Click on the "Fall Time" measurement field on the left side bar on the BERTScope and select "Detailed View". Record the mean Fall Time value (no need to wait since the fall time measurements were done simultaneously with the rise time measurements).
6. If the DUT claims to be capable of running at 3 Gb/s then repeat 1 through 5 of above to get both 1.5 Gb/s and 3 Gb/s measurements.
7. Calibrate the test set up by repeating 1 through 6 above using the same patterns, but generated by the pattern generator of the BERTScope connected via the short matched pair of cables in place of the iSATA receptacle to SMA Female Adapter and the DUT. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. The patterns are pre-loaded on the BERTScope in "View", then "Generator", click on the blue "Generator" box, "User Pattern", "Load User File" then "SATA II" to select a pattern.







When calibrating the BERTScope clock need to be used. By clicking on "Synthesizer" the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the "Outputs On/Off" button. The calibrated measurement values are the square root of the difference between the square of recorded time and the square of the calibration time measurements; t_{rise} = square root of ($t_{rise\_measured}^2 - t_{rise\_cal}^2$) and t_{fall} = square root of ($t_{fall\_measured}^2 - t_{fall\_cal}^2$).

Observable Results: The pass/fail criteria are:

- Each of the three measured Rise Time and three measured Fall Time values shall be less than 273 ps (0.41 UI) (for components when running at 1.5Gb/s)
- Each of the three measured Rise Time and three measured Fall Time values shall be less than 136 ps (0.41 UI) (for components claiming to be capable of running at 3Gb/s)

Possible Issues: When initiating via BIST; there is 50% chance that the correct LBP appear due to the two possible disparities that the DUT might interpret. The solution is merely to repeat step 6 until the right disparity is received.

Test Title: TSG-03 : Differential Skew

Purpose: Verify that the Device Under Test, DUT, meets the Differential Skew specification of section 7.2.2.3.4 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

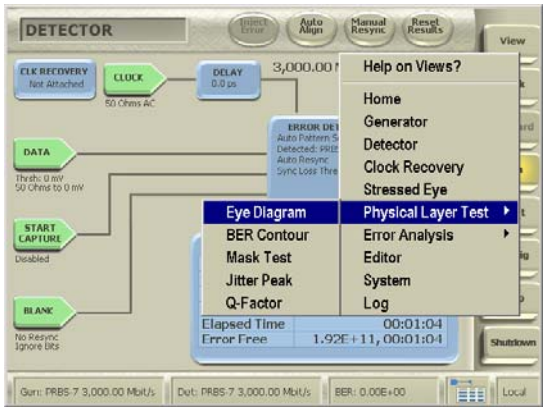
Last Modification: June 1, 2006

Discussion: This test is only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). Differential skew is measured as the difference between the mean of the rising edge in a single-ended eye diagrams of TX+ and the mean of the falling edge in a single-ended eye diagram of TX–, repeat the measurement this time measuring the difference between the mean of the rising edge in a single-ended eye diagrams of TX- and the mean of the falling edge in a single-ended eye diagram of TX+, finally compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement in accordance with section 7.4.12 of the Serial ATA revision 2.5.

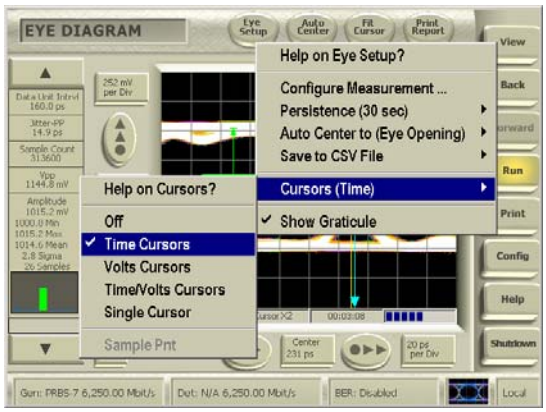
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

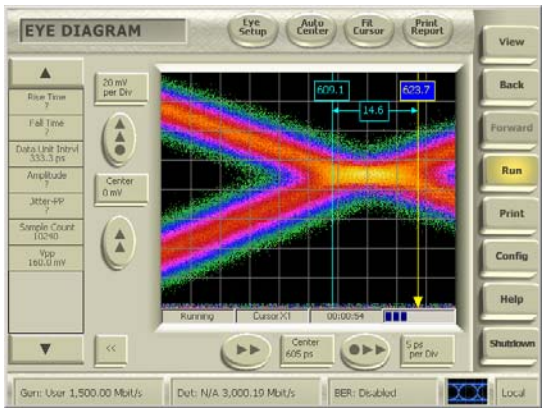
Test Procedure:

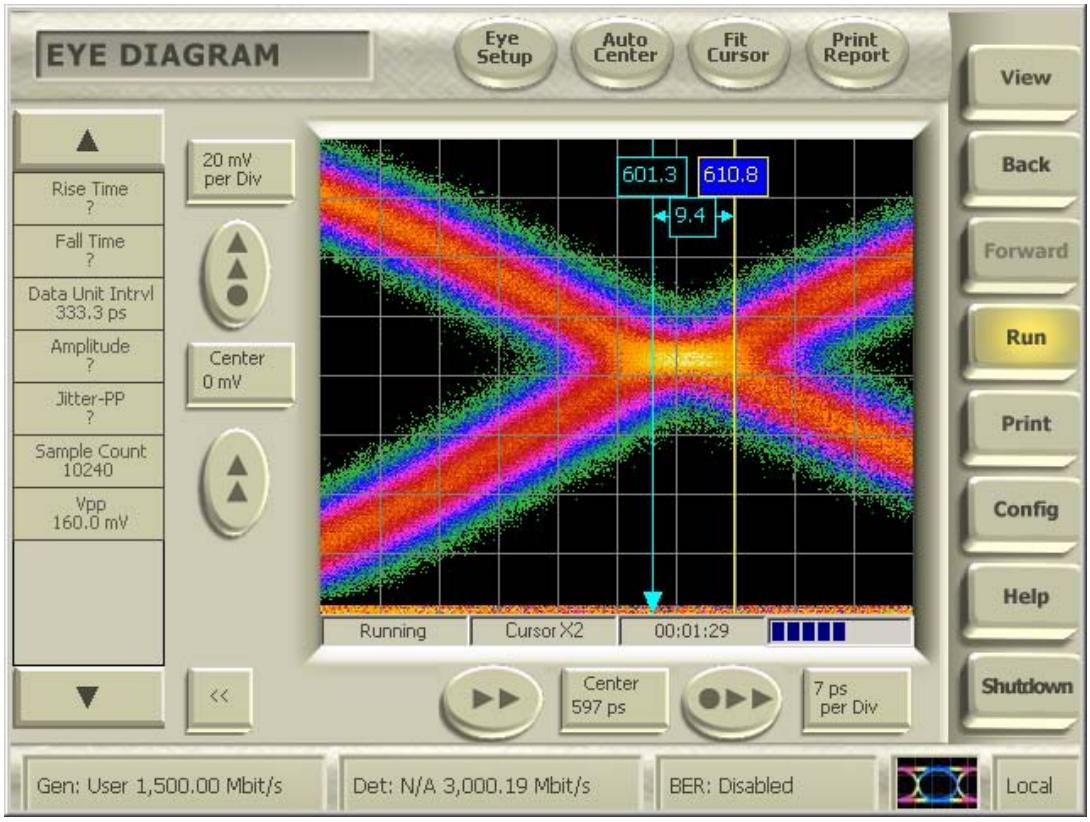
1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the DUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the DUT claims to be capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Click "Center xx mV" and set center voltage to 0 mV. Zoom in on the right most crossing by clicking on it and dragging it to the center of the display.



5. Click on “Eye Setup” on the BERTScope then “Cursors” and select “Time Cursors”. Place one cursor at the mid point of the falling edge. Place the second cursor near by and zoom in on the mid point by changing the time and/or voltage scale. It is desirable to allow the time scale to show a full 20 ps to either side of the mid point cursor.







6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Place the second cursor at the mid point of the rising edge. The delta between the first and second cursor is the mean skew between the falling edge of Data + and the rising edge of Data -.
8. Repeat 5 through 7 measuring from the rising edge of Data + to the falling edge of Data -.
9. Compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews.
10. The skew of the matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can be calibrated in any of two simple ways: One way is to switch the connections to the pins marked 6 and 5 of the iSATA receptacle and repeat above measurements 5 through 9, the calibrated value is then the average of the two computed differential skews; the other method is to calibrate per procedure in Appendix D and subtract the calibrated setup skew from the measured differential skew. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. Additionally the skew of the iSATA receptacle to SMA Female adapter, which is stated on the calibration sheet that comes with the adapter, should also be subtracted.
11. Repeat 2 through 9 with the DUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- t_{skewTX} measured shall be less than 20 ps for both HFTP and MFTP measurements.

Test Title: TSG-04 : AC Common Mode Voltage

Purpose: Verify that the Device Under Test, DUT, meets the AC Common Mode Voltage specification of section 7.2.2.3.5 of Serial ATA revision 2.5 while transmitting a specified patterns, namely MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent
- One passive power combiner, Weinschel 1515 or equivalent
- One first order low pass filter having a cutoff equal to the bitrate/2, namely 1.5 GHz.

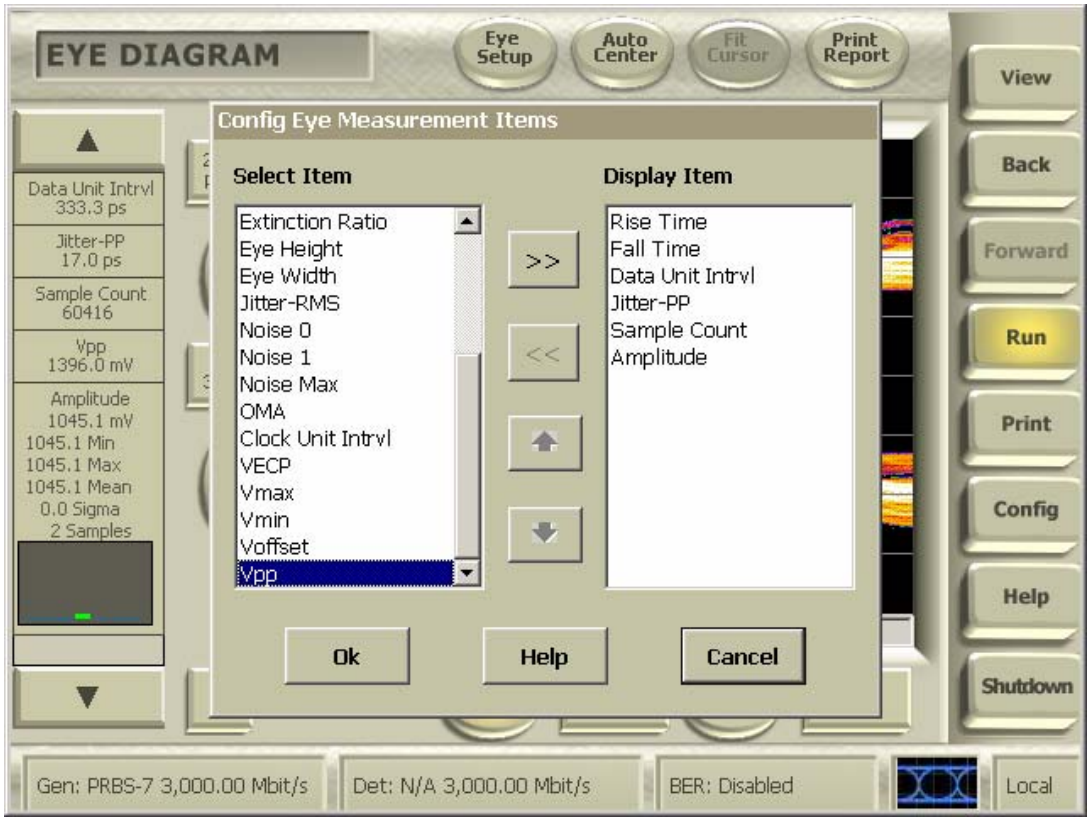
Last Modification: June 1, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The AC Common Mode Voltage is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Separate channels are used for TX+ and TX- through the CR 12500A where after they are terminated in a power combiner generating common mode (TX+ + TX-) / 2. This raw common mode shall be filtered with a first order filter having a cutoff equal to the bitrate / 2 to remove the noise contribution from the edge mismatches. The peak-to-peak voltage of the filter output is the AC Common Mode Voltage and shall remain below the specified limit in accordance with section 7.4.17 of the Serial ATA revision 2.5.

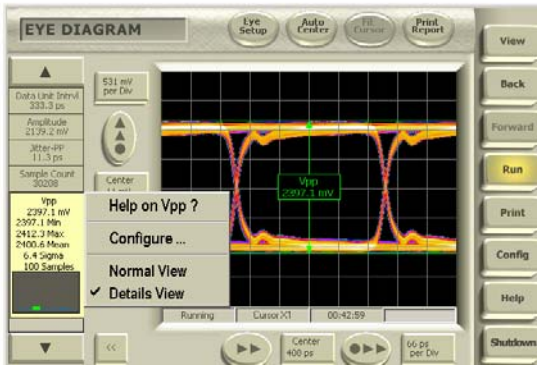
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the symmetrical input ports of the power combiner using the matched pair of cables. Connect the output of the power combiner to the low pass filter and connect the other end of the low pass filter to the Data Input + port on the BERTScope. Terminate the Data Input – port on the BERTScope with the 50 ohms termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the DUT transmitting the MFTP pattern at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram". Select "Eye Setup" then "Configure Measurement" and add "Vpp" to the list by highlighting "Vpp" then click on ">>" and "OK"



5. On the BERTScope, select “View” then “Physical Layer Test” and “Eye Diagram”. Select “Vpp” and “Detailed View”



6. Record the peak-to-peak voltage, which is the AC Common Mode Voltage.

Observable Results: The pass/fail criterion is:

- The measured AC Common Mode Voltage shall be less than 50 mVp-p.

Test Title: TSG-05 : Rise/Fall Time Imbalance

Purpose: Verify that the Device Under Test, DUT, meets the Rise/Fall Imbalance specification of section 7.2.2.3.9 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: June 1, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. In order to determine the imbalance, the single ended 20-80% rise and fall times of both TX+ and TX- shall be determined for a given pattern. Two imbalance values for that pattern are then determined by the two equations:

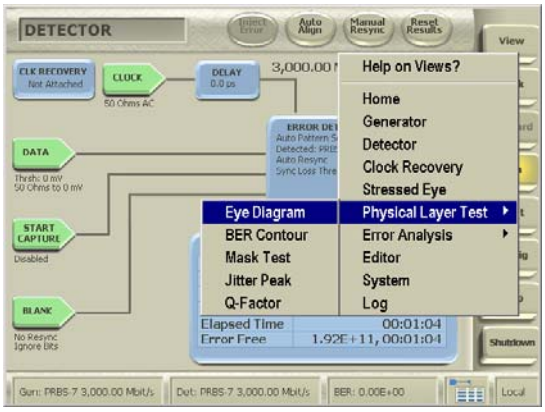
absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2

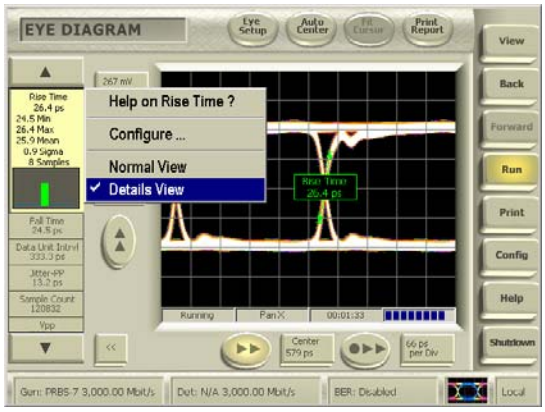
according to section 7.4.16 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR12500A, choose the pre-stored selection: "SATAII (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again.
2. Initiate the DUT transmitting the HFTP pattern (D10.2) at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Right click on the "Rise Time" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reach at least 10,000 and record the mean Rise Time value of TX+.





5. Right click on the "Fall Time" measurement field on the left side bar on the BERTScope and select "Detailed View". Record the mean Fall Time value of the TX+ (no need to wait since the fall time measurements were done simultaneously with the rise time measurements).
6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Repeat 4 through 5.measuring the Rise and Fall times of TX–.
8. Compute the two imbalance values for the pattern determined by the two equations:

   absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
   absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2.

9. Repeat 2 through 8 with the DUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- Each pair of the two Rise/Fall Time Imbalances measured shall be less than 20% for both HFTP and MFTP measurements.

Test Title: TSG-06 : Amplitude Imbalance

Purpose: Verify that the Device Under Test, DUT, meets the Amplitude Imbalance specification of section 7.2.2.3.10 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: June 1, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. In order to determine the imbalance, the single ended amplitudes of both TX+ and TX- shall be determined for a given pattern. The imbalance value for that pattern is then calculated by the equation:

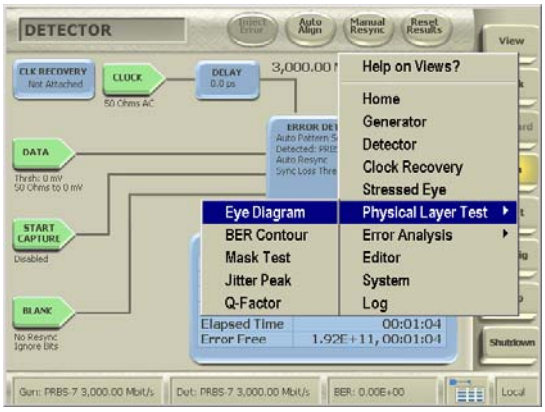
absolute value (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2

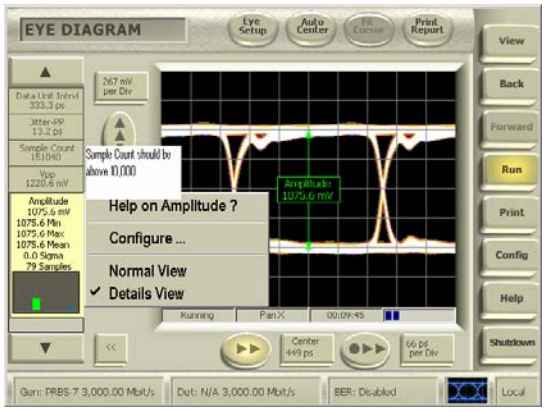
where all amplitudes are determined according to section 7.4.15 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the DUT in BIST T,S,A mode transmitting the HFTP pattern (D10.2) at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the DUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Right click on the "Amplitude" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reached at least 10,000 and record the mode amplitude value of TX+.





5. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
6. Repeat 4 through 5.measuring the Amplitude of TX–.
7. Compute the imbalance value for the pattern determined by the equation: absolute value of (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2
8. Repeat 2 through 7 with the DUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- The mean Amplitude Imbalances measured shall be less than 10% for both HFTP and MFTP measurements.

Test Title: TSG-09: TJ at Connector, Data, 250 UI

Purpose: Verify that the Device Under Test, DUT, meets the TJ specification of section 7.2.2.3.11 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 1.5 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

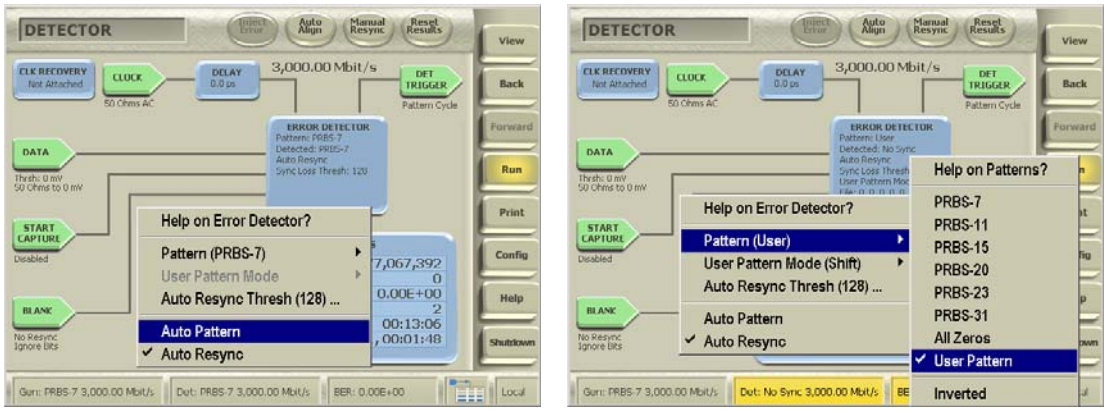
Last Modification: June 1, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at 1.5Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-09 and TSG-10 using the BERT method according to section 7.4.8 of the Serial ATA revision 2.5 using the methodology required by the following text of the Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc: "For this test, the methodology of obtaining the results must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing."

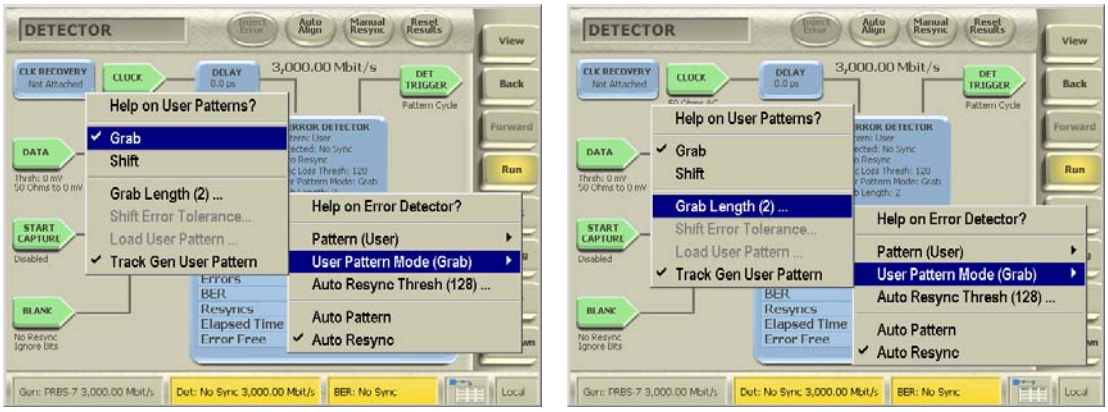
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

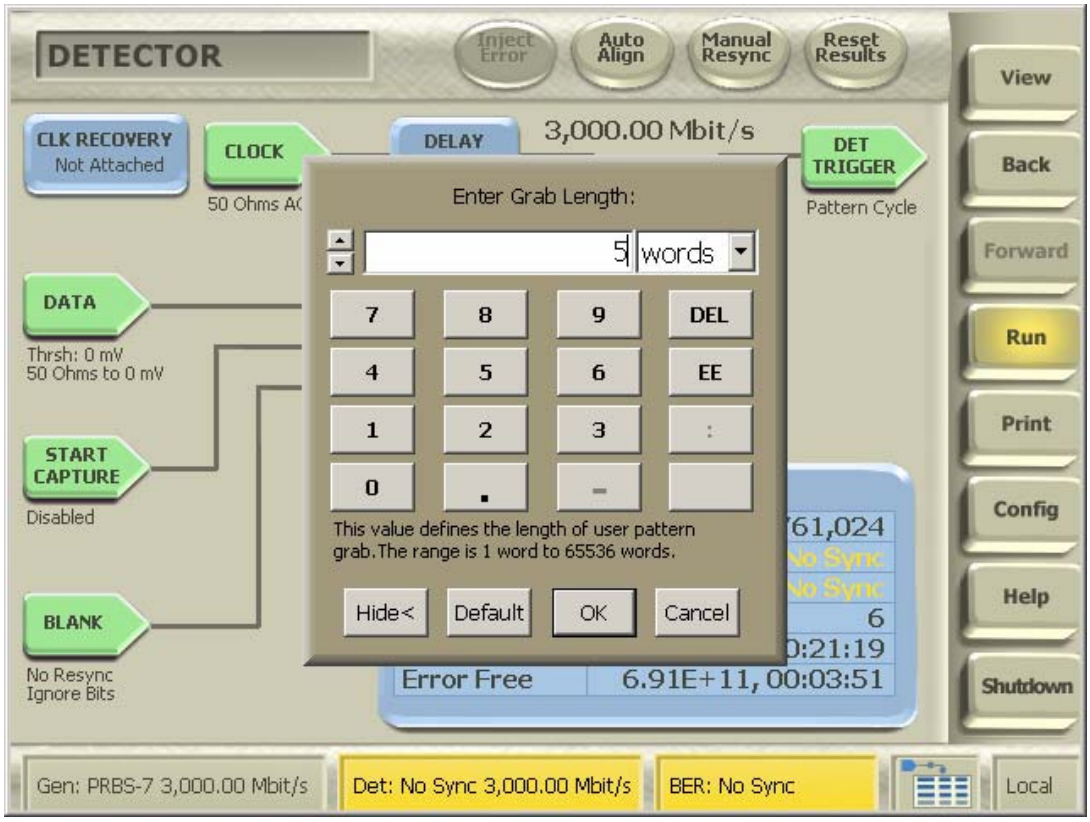
1. On CR 12500A, choose the pre-stored selection: "SATA1 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".



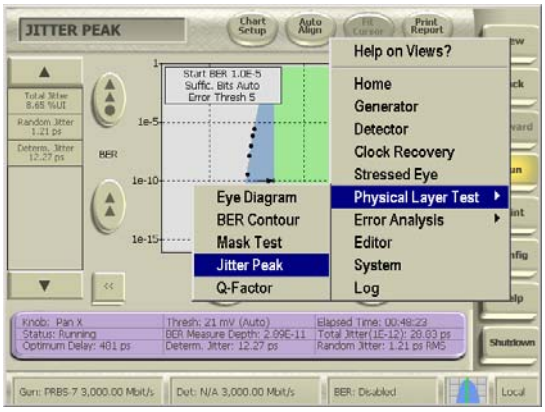
3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

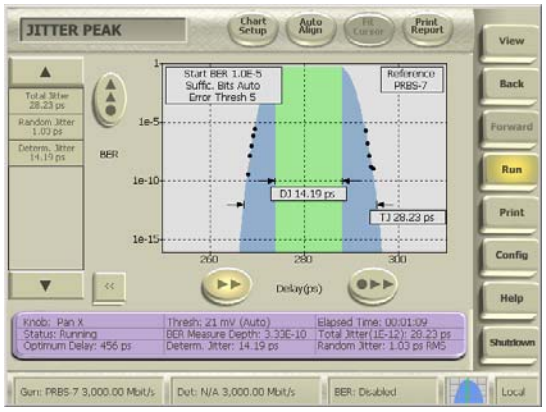


Enter “5” setting the grab length to 5 words and click “OK”.

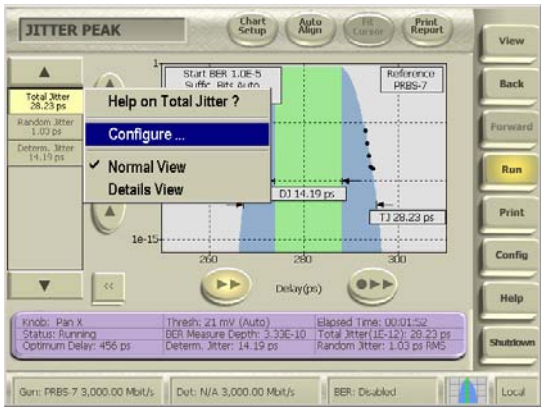


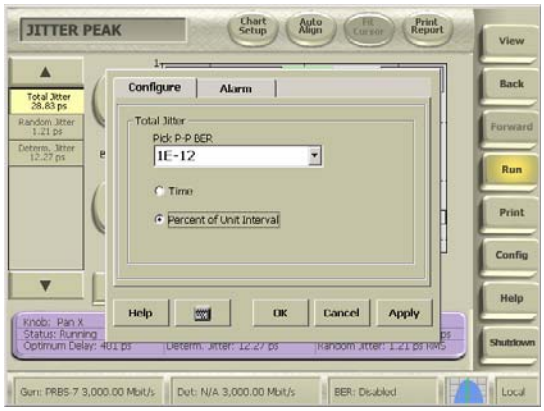
4. Initiate the DUT transmitting the HFTP pattern using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the DUT to the iSATA receptacle
6. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI (DJ may be recorded at the same time as this completes the TSG-10 measurement as well).



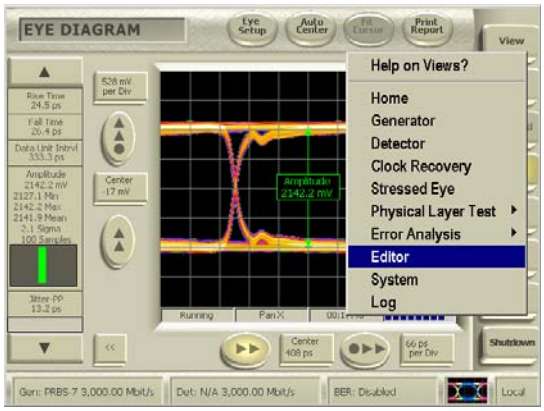


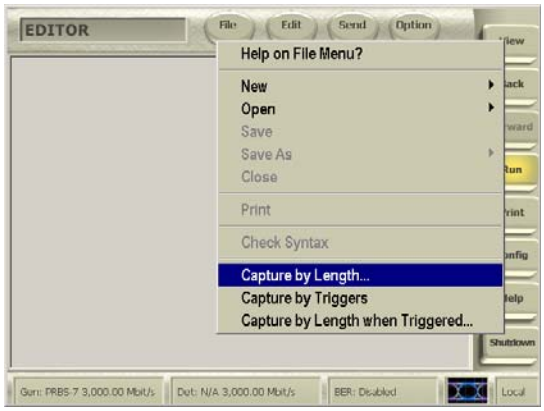
The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





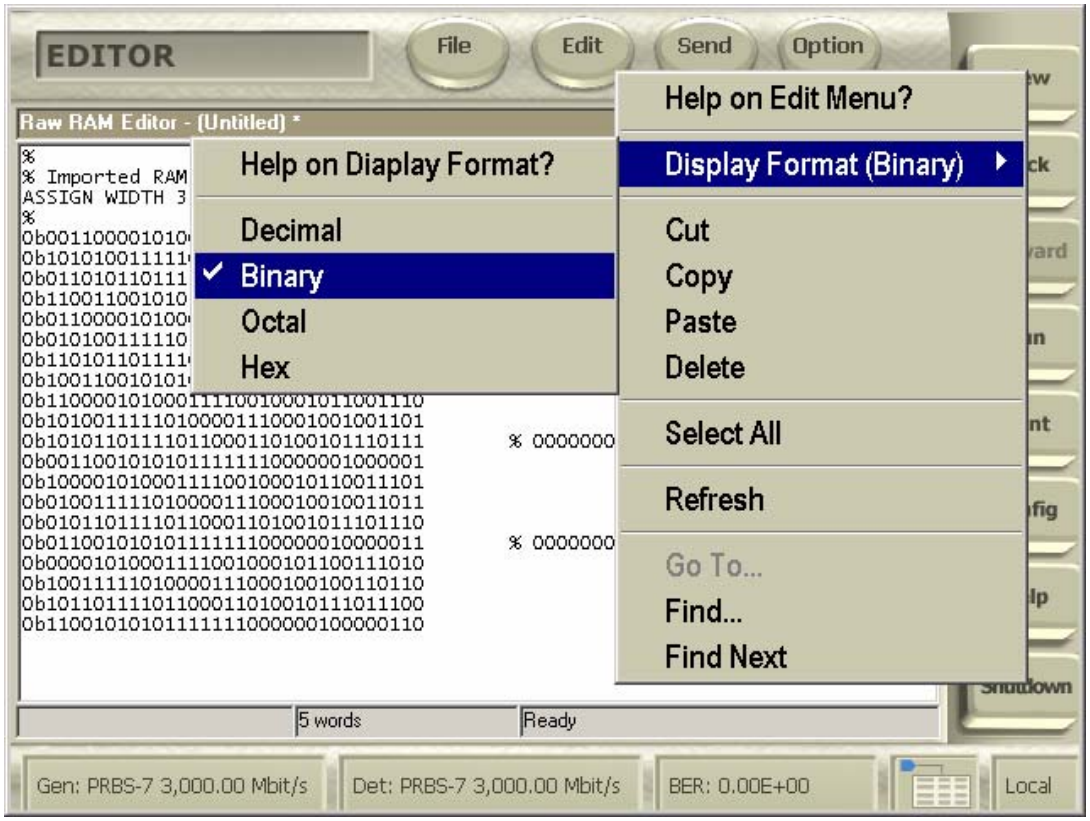
7. Repeat 4 through 6 with the DUT initiated transmitting the LBP pattern. Verify that the right disparity of the LBP is received by selecting “View” then “Editor” on the BERTScope. Click “File” then “Capture By Length”.





8. Click “OK” to override RAM. Enter “5” words and click “OK”.

Toggle the view to binary by click on "Edit" then "Display Format" and "Binary". Verify that the pattern contains the "00001000" sequence.



9. Repeat 4 through 6 with the DUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criterion is:

- TJ measured must be less than 0.47 UI at 1.5 Gb/s for each of the test patterns.

Possible Issues: When initiating via BIST; there is 50% chance that the correct LBP appear due to the two possible disparities that the DUT might interpret. The solution is merely to repeat step 6 until the right disparity is received.

Test Title: TSG-10: DJ at Connector, Data, 250 UI

Purpose: Verify that the Device Under Test, DUT, meets the DJ specification of section 7.2.2.3.11 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 1.5 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

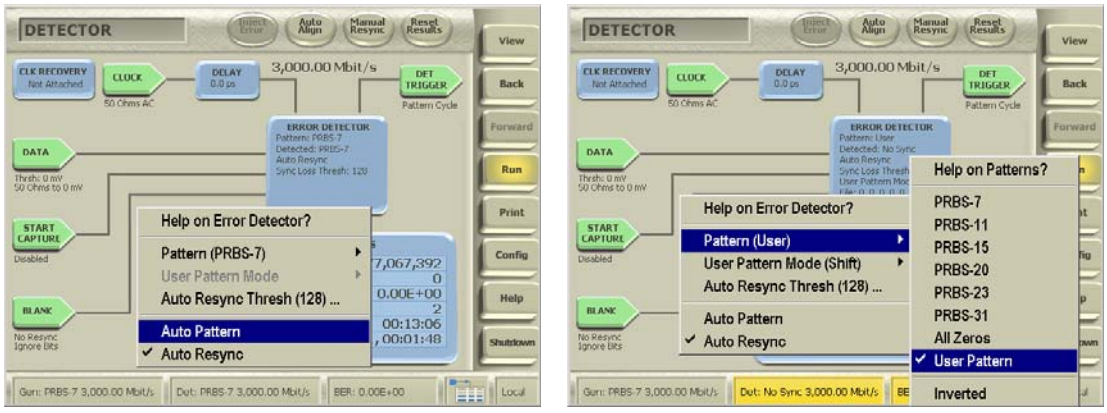
Last Modification: June 1, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at 1.5Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-09 and TSG-10 using the BERT method according to section 7.4.8 of the Serial ATA revision 2.5 using the methodology required by the following text of the Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc: "For this test, the methodology of obtaining the results must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing."

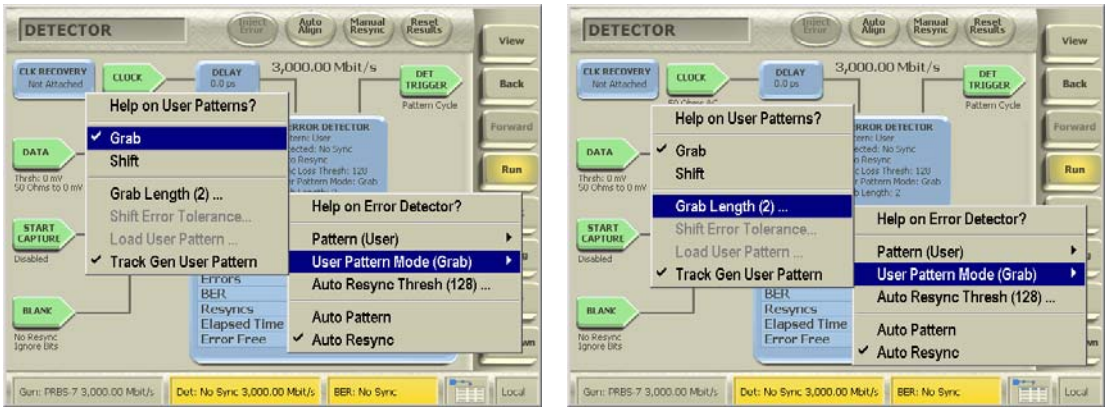
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

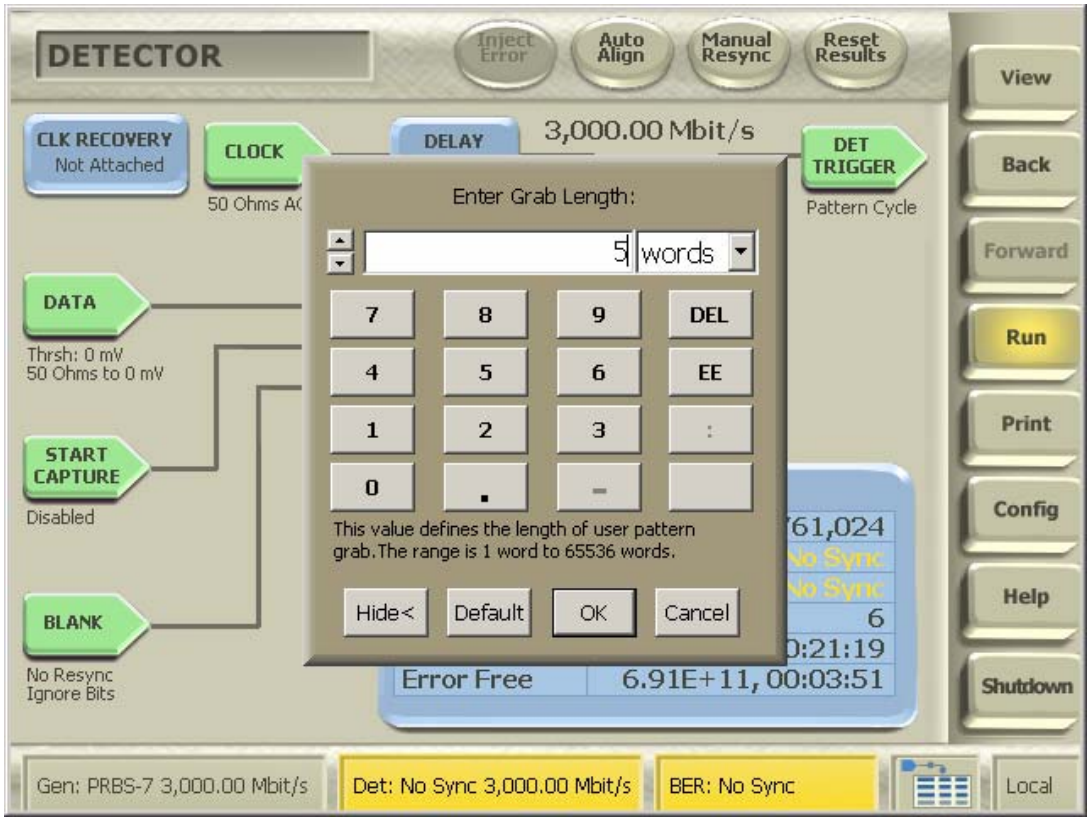
1. On CR 12500A, choose the pre-stored selection: "SATA1 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".



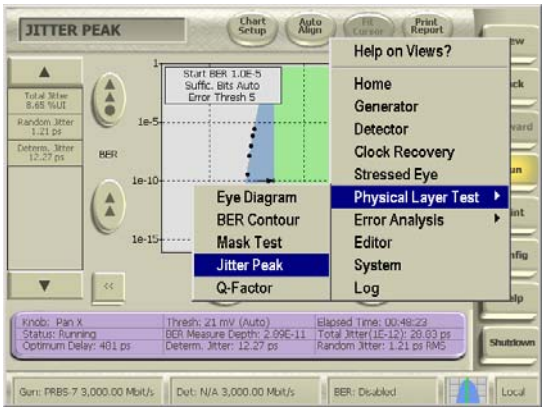
3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

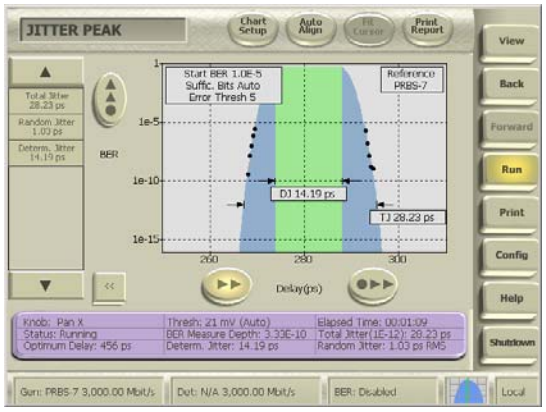


Enter “5” setting the grab length to 5 words and click “OK”.

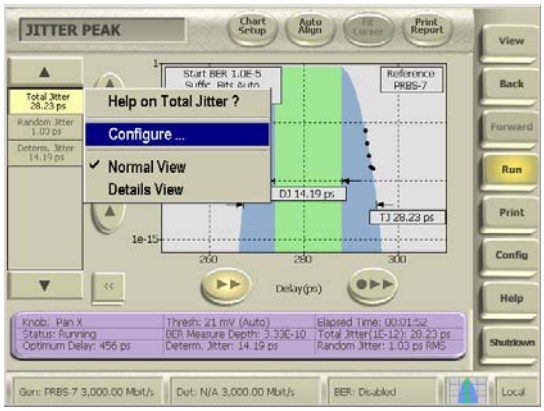


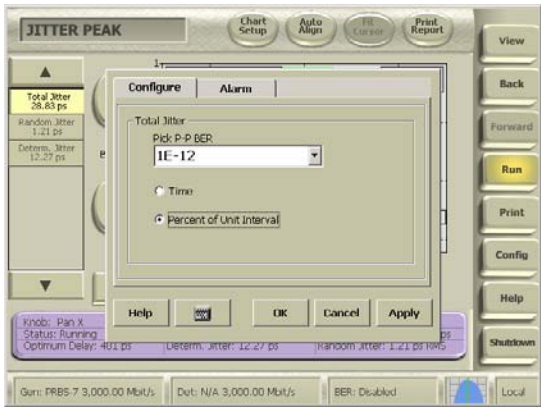
4. Initiate the DUT transmitting the HFTP pattern using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the DUT to the iSATA receptacle
6. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the DJ value in UI (TJ may be recorded at the same time as this completes the TSG-09 measurement as well).



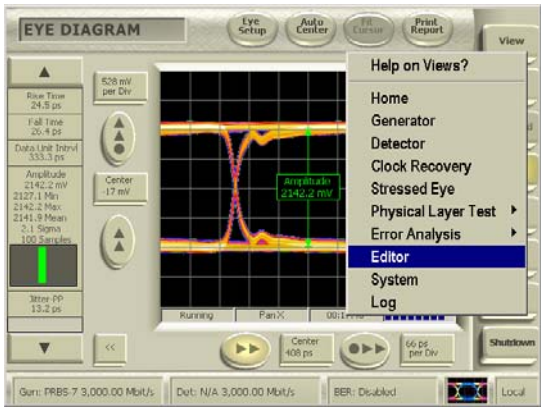


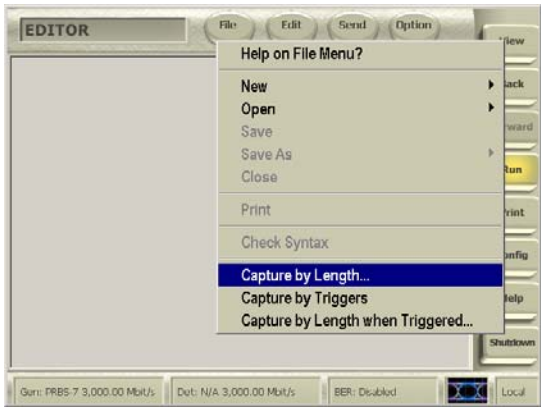
The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





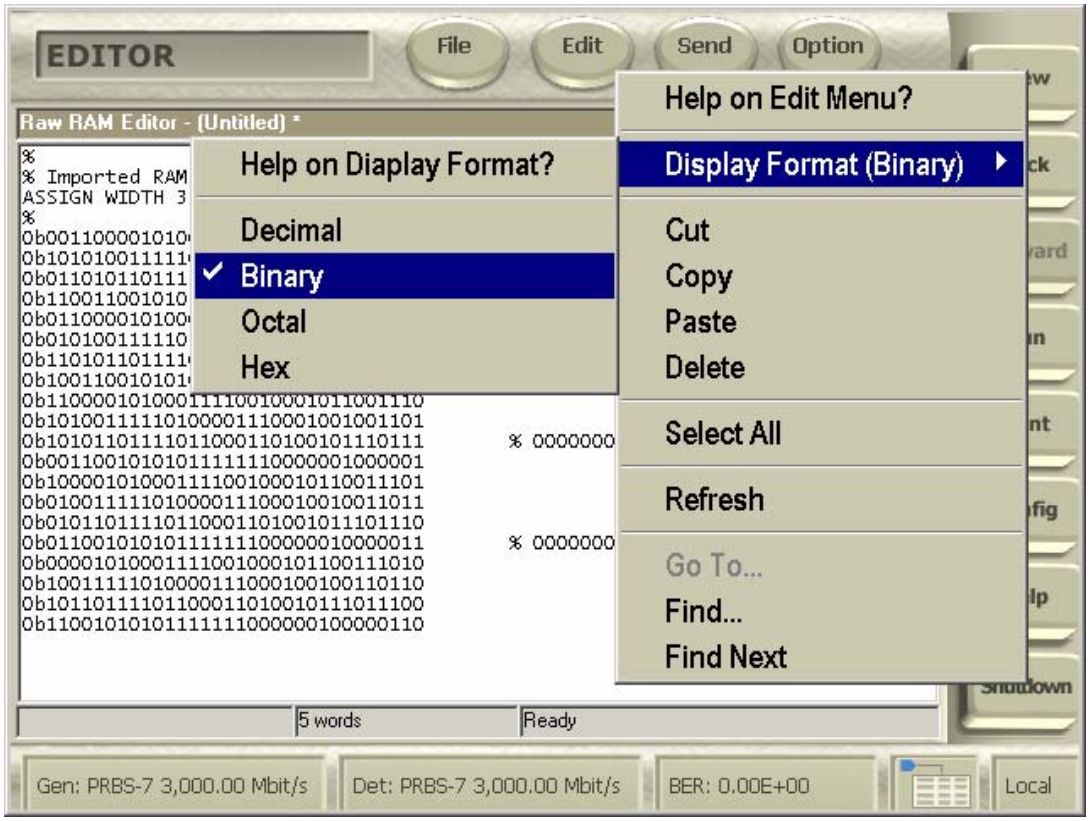
7. Repeat 4 through 6 with the DUT initiated transmitting the LBP pattern. Verify that the right disparity of the LBP is received by selecting “View” then “Editor” on the BERTScope. Click “File” then “Capture By Length”.





8. Click “OK” to override RAM. Enter “5” words and click “OK”.

Toggle the view to binary by click on "Edit" then "Display Format" and "Binary". Verify that the pattern contains the "00001000" sequence.



9. Repeat 4 through 6 with the DUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criterion is:

- DJ measured must be less than 0.22 UI at 1.5 Gb/s for each of the test patterns.

Possible Issues: When initiating via BIST; there is 50% chance that the correct LBP appear due to the two possible disparities that the DUT might interpret. The solution is merely to repeat step 6 until the right disparity is received.

Test Title: TSG-11: TJ at Connector, Clock, 500

Purpose: Verify that the Device Under Test, DUT, meets the TJ specification of section 7.2.2.3.12 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 3 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

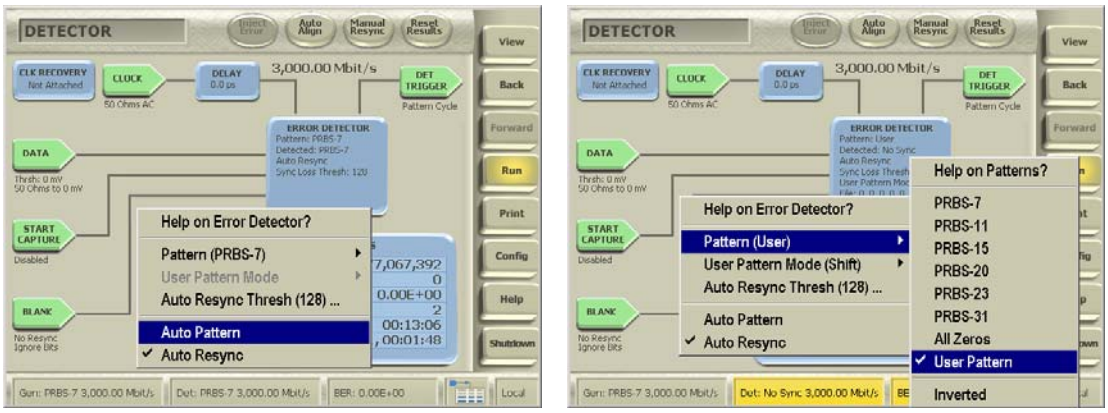
Last Modification: June 1, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-11 and TSG-12 using the BERT method according to sections 7.4.6 and 7.4.8 of the Serial ATA revision 2.5.

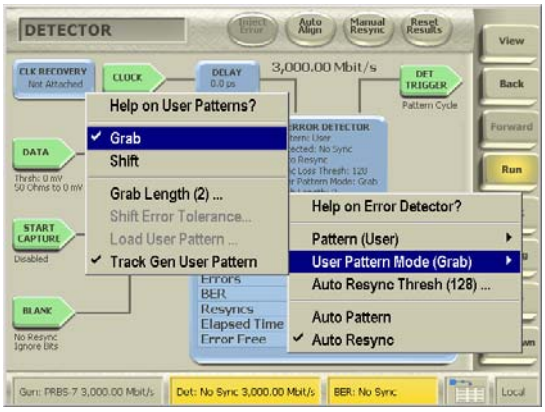
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

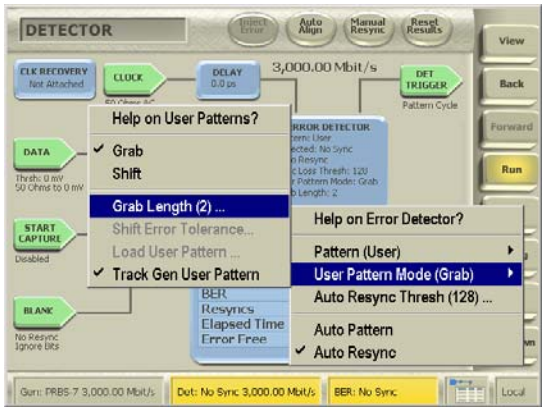
Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".

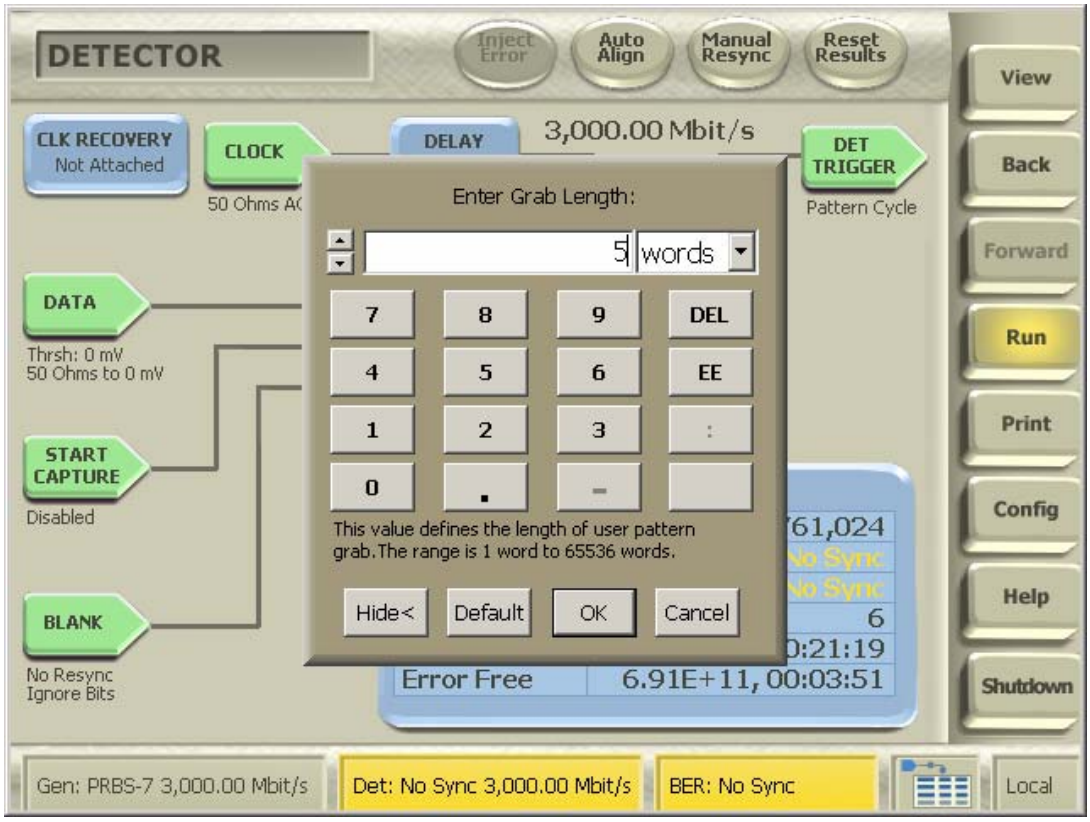


3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

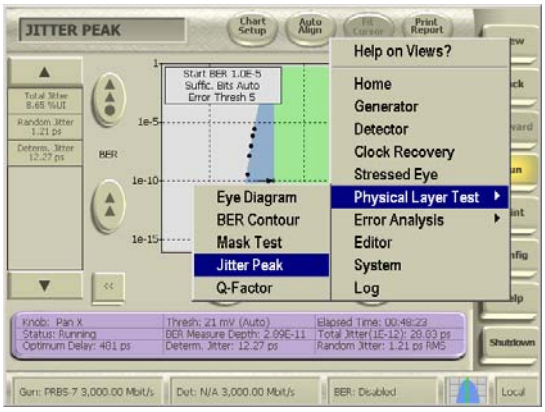


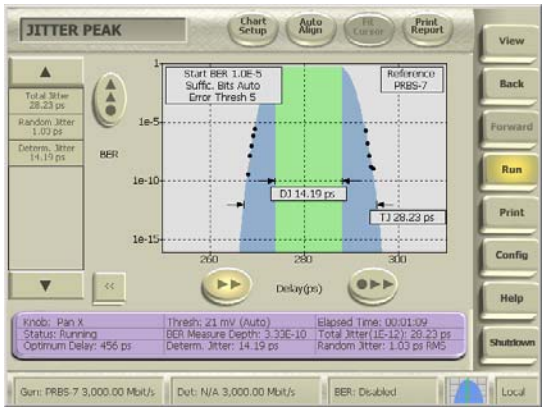


Enter “5” setting the grab length to 5 words and click “OK”.

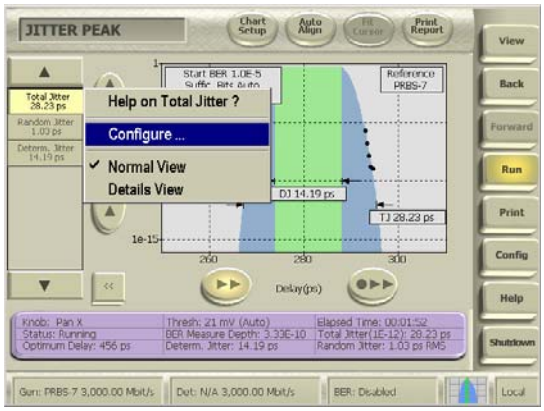


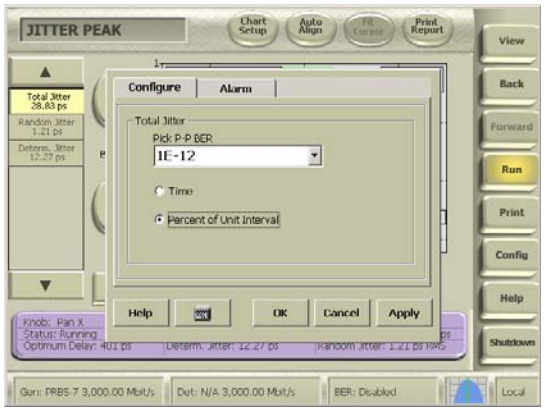
4. Initiate the DUT transmitting the HFTP pattern at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the DUT to the iSATA receptacle
6. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI (DJ may be recorded at the same time as this completes the TSG-12 measurement as well).



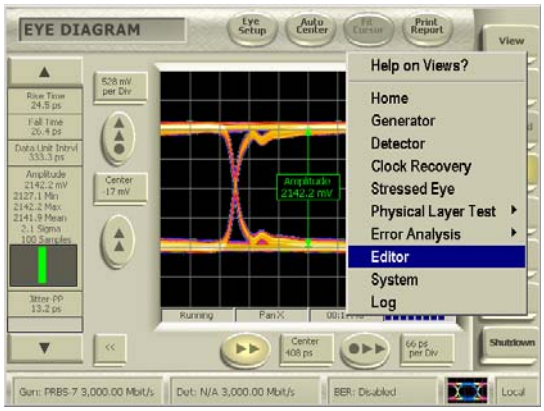


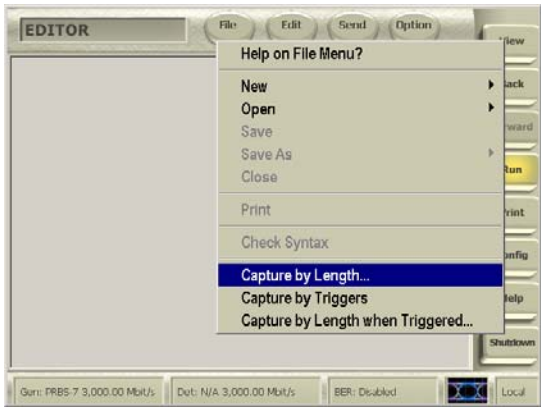
The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





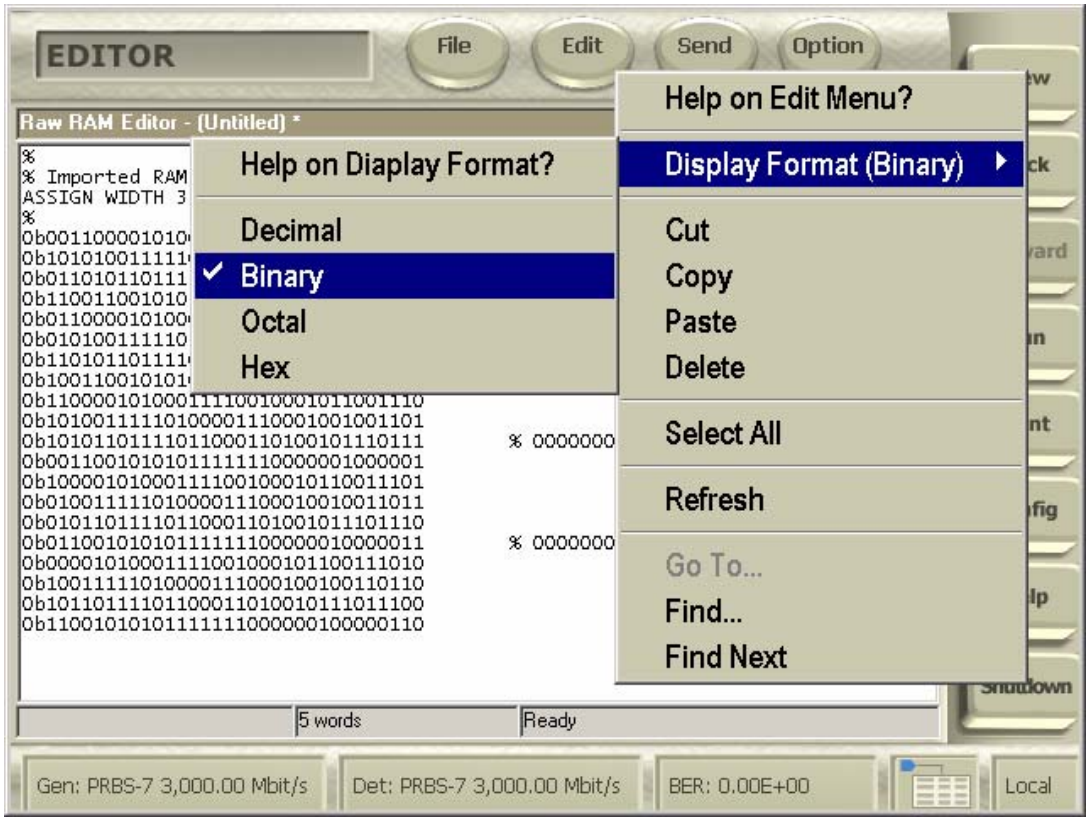
7. Repeat 4 through 6 with the DUT initiated transmitting the LBP pattern. Verify that the right disparity of the LBP is received by selecting “View” then “Editor” on the BERTScope. Click “File” then “Capture By Length”.





8. Click “OK” to override RAM. Enter “5” words and click “OK”.

Toggle the view to binary by click on "Edit" then "Display Format" and "Binary". Verify that the pattern contains the "00001000" sequence.



9. Repeat 4 through 6 with the DUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- TJ measured must be less than 0.37 UI at 3 Gb/s for each of the test patterns.

Possible Issues: When initiating via BIST; there is 50% chance that the correct LBP appear due to the two possible disparities that the DUT might interpret. The solution is merely to repeat step 6 until the right disparity is received.

Test Title: TSG-12: DJ at Connector, Clock, 500

Purpose: Verify that the Device Under Test, DUT, meets the DJ specification of section 7.2.2.3.12 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 3 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

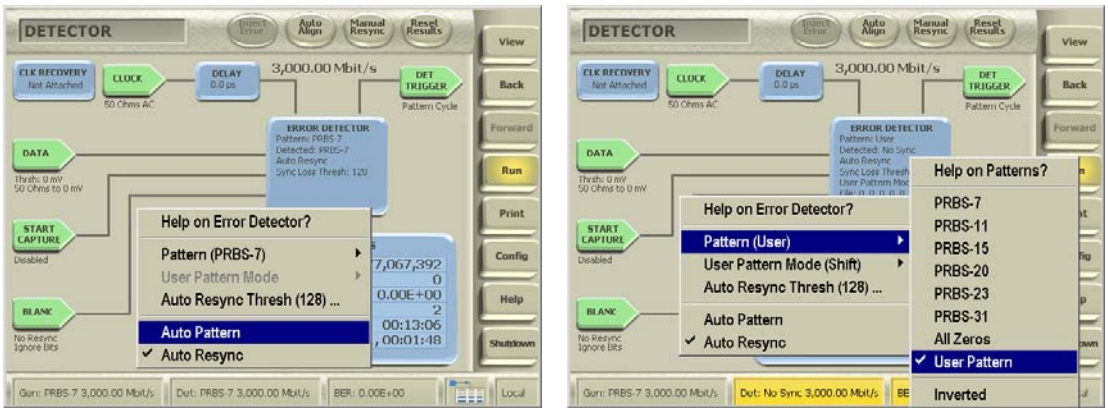
Last Modification: June 1, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-11 and TSG-12 using the BERT method according to sections 7.4.6 and 7.4.8 of the Serial ATA revision 2.5.

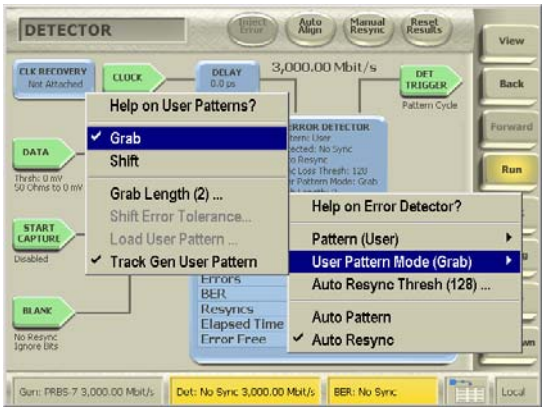
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

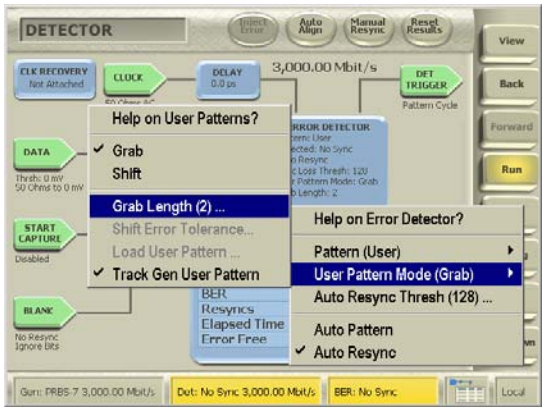
Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".

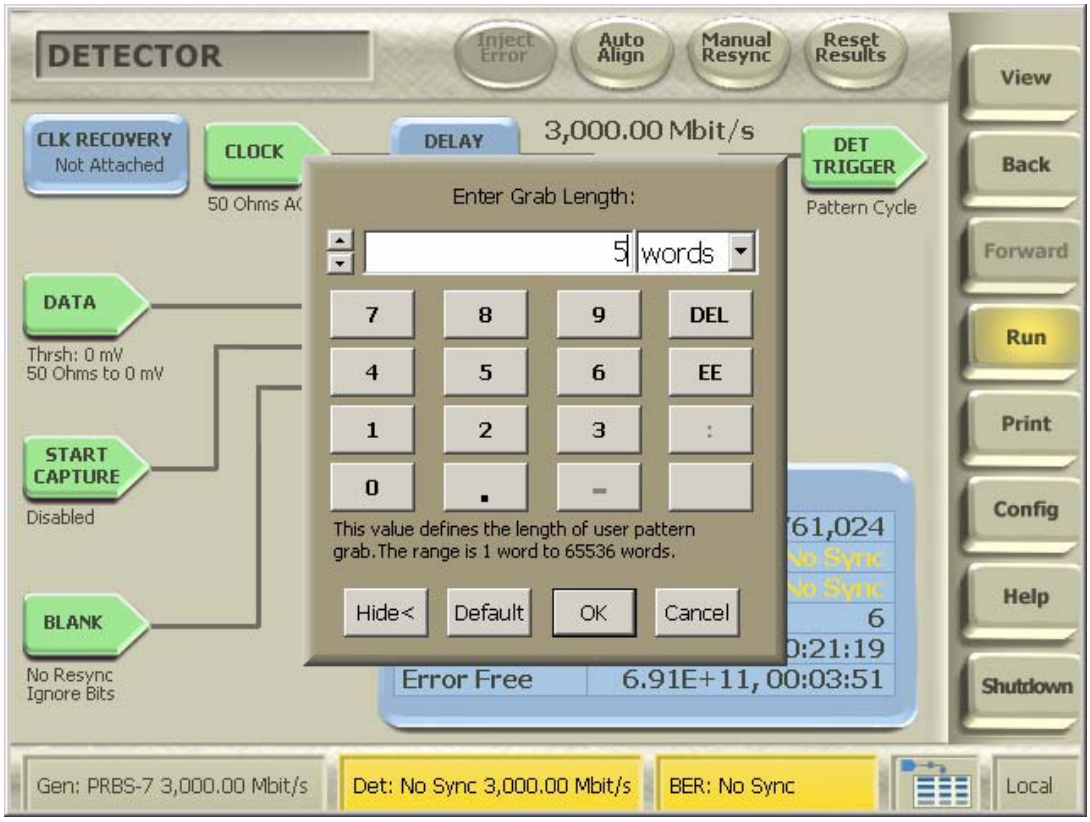


3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

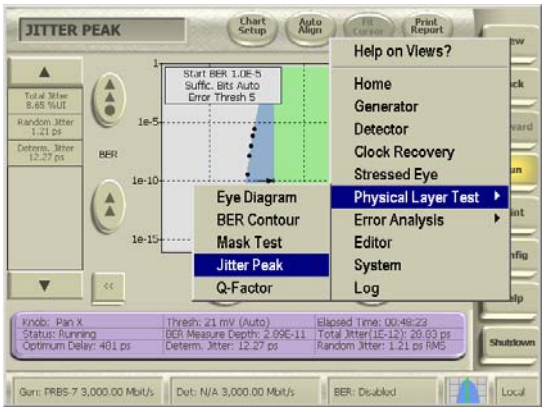


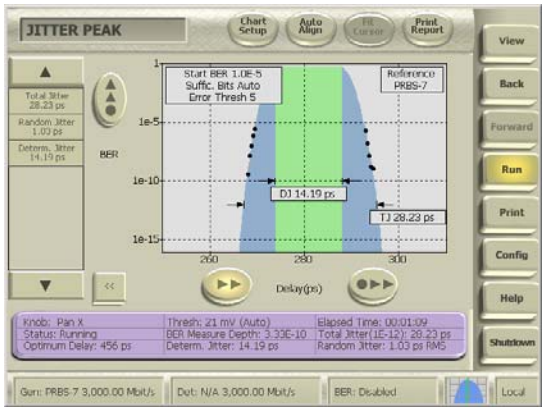


Enter “5” setting the grab length to 5 words and click “OK”.

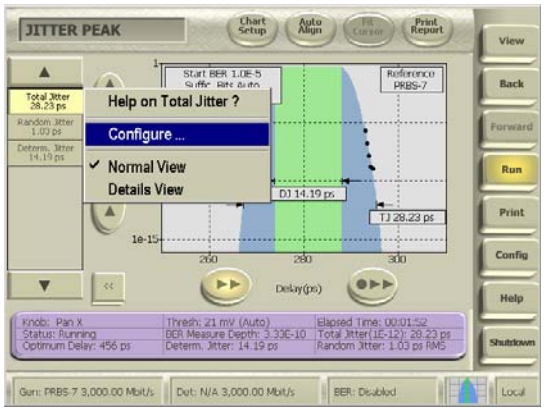


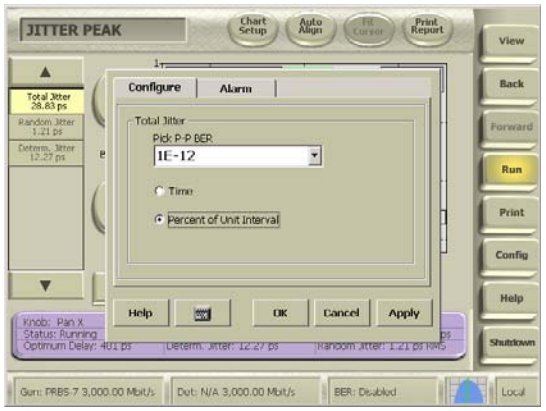
4. Initiate the DUT transmitting the HFTP pattern at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the DUT to the iSATA receptacle
6. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the DJ value in UI (TJ may be recorded at the same time as this completes the TSG-11 measurement as well).



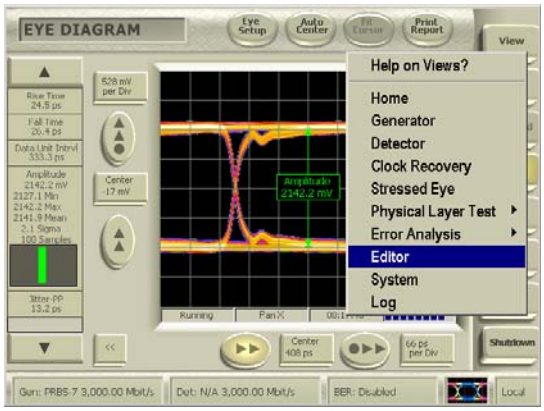


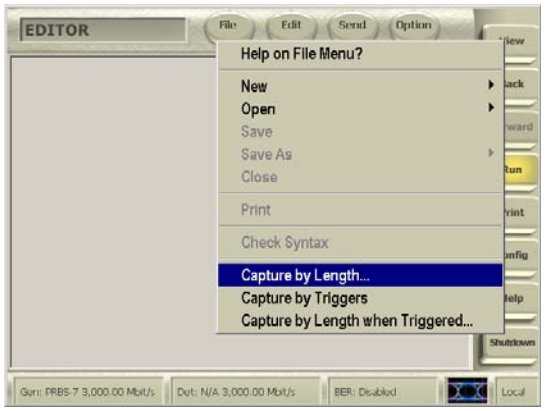
The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





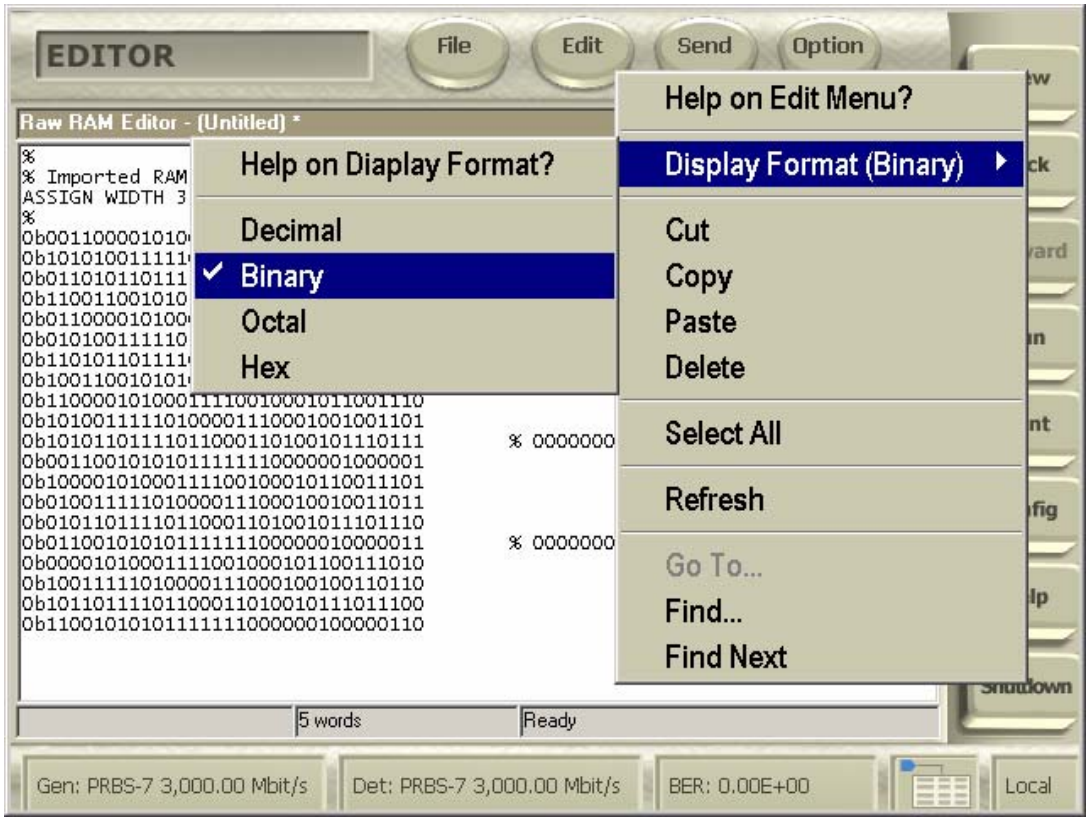
7. Repeat 4 through 6 with the DUT initiated transmitting the LBP pattern. Verify that the right disparity of the LBP is received by selecting “View” then “Editor” on the BERTScope. Click “File” then “Capture By Length”.





8. Click “OK” to override RAM. Enter “5” words and click “OK”.

Toggle the view to binary by click on "Edit" then "Display Format" and "Binary". Verify that the pattern contains the "00001000" sequence.



9. Repeat 4 through 6 with the DUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- DJ measured must be less than 0.19 UI at 3 Gb/s for each of the test patterns.

Possible Issues: When initiating via BIST; there is 50% chance that the correct LBP appear due to the two possible disparities that the DUT might interpret. The solution is merely to repeat step 6 until the right disparity is received.

Appendix A:

Initiation of DUT using BIST modes.

Purpose: The DUT is placed in one of two BIST modes, namely T+S+A or L and programmed with the desired test pattern as an initiation before the BERTScope measurements.

References:

1. Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf
2. U-Link Operating Help Files

Resource Requirements: Intel ICH7 based computer with U-Link DriveMaster 2006 software version 3.0.198e or later.

Last Modification: February 11, 2006

Test Setup: Intel ICH7 based computer with an iSATA cable.

Test Procedure:

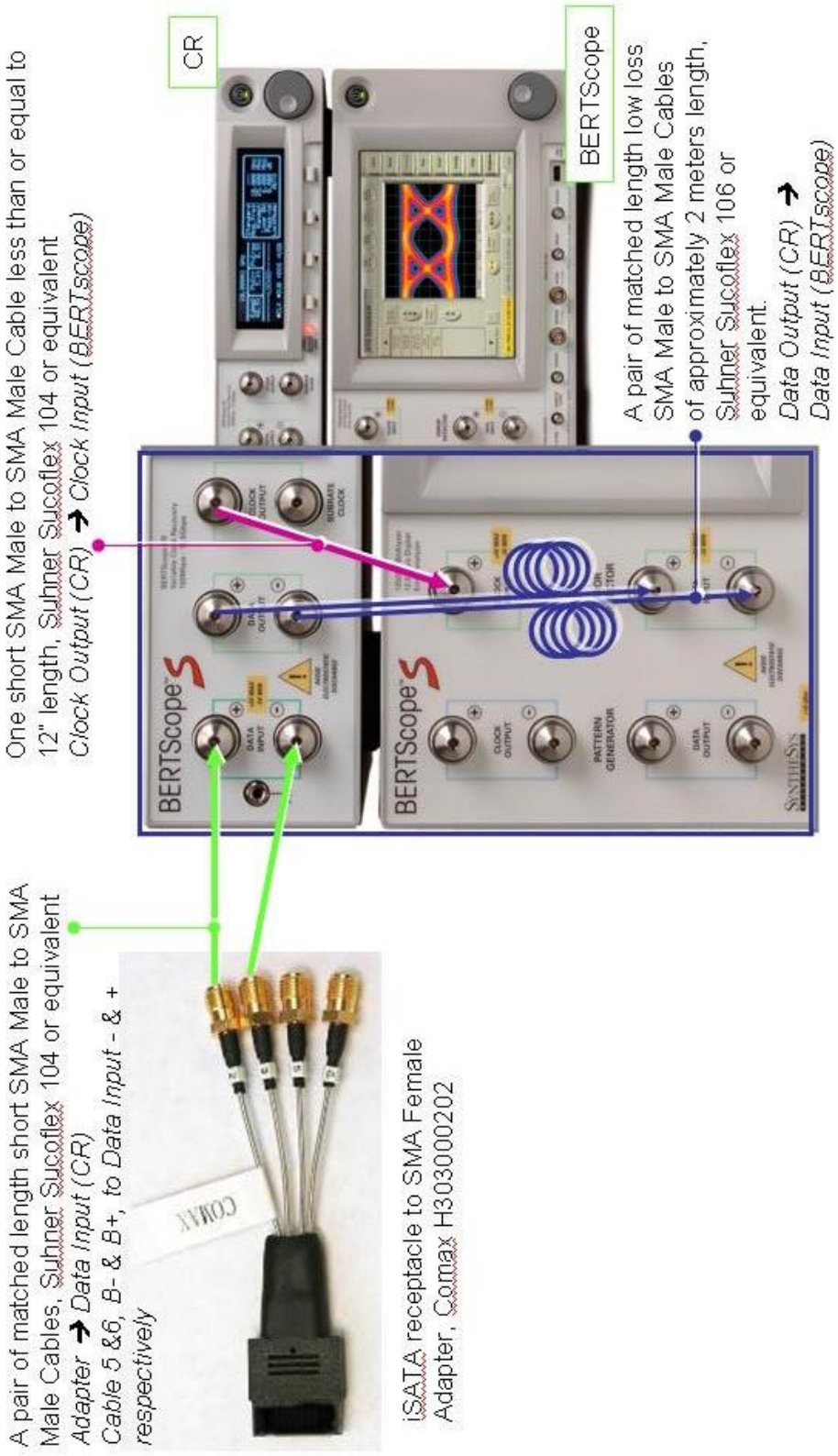
1. Connect DUT to the ICH7 using the SATA cable.
2. Start the U-Link program
3. Click “Power Up” and observe the power supply spin up. Leave it on.
4. Click “CtlSATA”
5. Click COMRESET and observe that COMRESET was received on the log on the right side of the DriveMaster window..
6. Select the appropriate data rate “1” or “2” and observe that the “RDSTATUS” displays “00000113” or “00000123” for 1.5 Gb/s and 3 Gb/s respectively.
7. Select the appropriate “BIST mode T, S, A” for PHY and TSG Testing or “BIST mode L” for RTL Testing
8. When initiating PHY or TSG tests; select the desired pattern from the list.
9. Click “BIST” and observe that “BIST FIS SUCEEDED” is displayed in the lower left corner of the SATA Control Panel.
10. DUT should now be ready for test.

Possible Issues: Some DUTs may require sequences of ALIGN words to be transmitted when switched from the U-Link initiation to the BERTScope set-up when doing RTL tests. This can be accomplished by using the pattern sequencing on the BERTScope having the A pattern be ALIGNs followed by the B pattern being the desirable test pattern. AB patterns are pre-stored on the BERTScope for this purpose.

If the DUT lacks support of physical disconnect then a pair of couplers or power dividers are needed to be able to communicate with the DUT using the U-Link software on the computer and the BERTScope without physical disconnect.

Appendix B:

Serial ATA Interoperability Program Unified Test Setup using BERTScope[1].



[1]Setup including cables and adaptors to have return loss per SATA specifications and be deskewed to within 1 ps.

Appendix C:

Calibration of Voltage versus Frequency Sensitivity of the Frequency Tracking output on the CR12500A Clock Recovery Instrument.

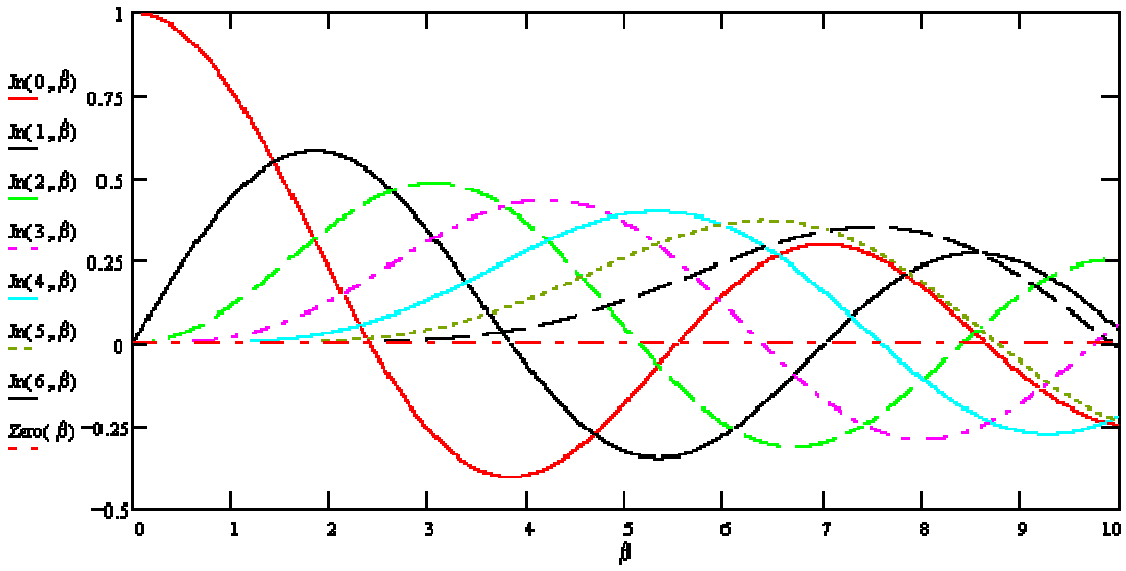
Purpose: Calibration of the CR 12500A frequency tracking output allows conversion from voltage measured on the output to the frequency deviation desired in the PHY03 spread spectrum frequency deviation measurement.

Resource Requirements:

- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One short SMA Male to SMA Male Cable, Suhner Sucoflex 104 or equivalent
- One BNC Male to BNC Male Cable, Suhner RG58/BNCm/BNCm/1000r or equivalent
- One SMA Male to BNC Female adaptor, Suhner 33SMA-BNC-50-1 or equivalent
- One Oscilloscope, Tektronix TDS3064B or equivalent having a bandwidth greater than 1 MHz
- Two 50 ohms terminations, SUHNER 65SMA-50-0-1 or equivalent (unless one BERTScope 7500 or BERTScope 12500 is present with a pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent)
- One 3 GHz signal generator with frequency modulation, FM, capabilities, Gigatronics 2408B with option 26 or equivalent
- One 3 GHz spectrum analyzer, Tektronix RSA2203A or equivalent.

Last Modification: June 1, 2006

Discussion: The clock recovery instrument tracks the low frequency modulation of the input within a loop bandwidth and range of damping factors per Serial ATA version 2.5. The clock recovery instrument further provides a rear panel output with a voltage proportional to the frequency deviation of the tracking signal. Calibration is performed by injecting a signal at 1.5 GHz and 3 GHz respectively with known frequency modulation and deviation into the CR 12500A and oscilloscope combination and measure the deviation voltage on the oscilloscope. The preferred sinusoidal modulation frequency is 300 kHz in order to be similar in frequency to the SSC signals (this would be close to the ninth harmonic as may be found in a triangular waveform of the 33 kHz) while being as large as possible in order to get a significant frequency deviation. The frequency modulated signal is initially injected into and viewed on a spectrum analyzer while the frequency deviation is adjusted until the carrier disappears. The carrier power disappears when the Bessel Function of zero order, called $J_n(0,\beta)$, equals zero. This happens when the modulation index, called β, which is the frequency deviation divided by the modulation frequency, equals either of the following: 2.4048; 5.5201; 8.6537; 11.7915; 14.9309; 18.0711 or larger values as shown on the graph:



The preferred setting of the frequency deviation is at the value corresponding to the highest possible modulation index allowed by the signal generator that provides a carrier null, $J_n(0,\beta) = 0$, For example β = 11.7915, which corresponds to a frequency deviation of 11.7915 x 300 kHz = 3537.45 kHz (or peak-to-peak deviation of 7074.9 kHz). or β = 5.5201, which corresponds to a frequency deviation of 5.5201 x 300 kHz = 1656.03 kHz (or peak-to-peak deviation of 3312.06 kHz).The calibration factor is the peak-to-peak frequency deviation of the known modulation divided by the peak-to-peak deviation voltage measured on the oscilloscope.

Calibration Setup: Initially connect the output of the signal generator to the input of the spectrum analyzer. Set up the signal with known frequency deviation as per the test procedure then connect the output of the signal generator using the same cable to the input of Data Input + port of the CR 12500A. Connect the CR 12500A rear panel output marked Phase Error to the input port on the Oscilloscope. Make sure that the Data Output + and - ports of the CR12500A are either connected to the Data Input + and – ports of the BERTScope using the matched pair of cables or terminated using the 50 ohms terminations..

Calibration Procedure:

1. Set the output frequency of the signal generator to 1.5 GHz and a sinusoidal modulation frequency to 300 kHz.
2. Connect the output of the signal generator to the input of the spectrum analyzer.
3. While looking at the spectrum on the spectrum analyzer, adjust the modulation amplitude on the signal generator starting from the minimum deviation until the carrier disappears, this ought to be at the first null having a modulation index, β, of 2.40. Continue to increase the deviation until the null with the desired β has been reached. The peak-to-peak frequency deviation is now exactly 2 x β x 300 kHz , record this value.
4. Apply the output of the signal generator to the Data Input + port of the CR 12500A.
5. Record the peak-to-peak voltage deviation measured on the oscilloscope.
6. Calculate the calibration factor as the peak-to-peak frequency deviation divided by the peak-to-peak voltage deviation.
7. Repeat steps 2 through 6 above with the output frequency of the signal generator set to 3.0 GHz and a sinusoidal modulation frequency at 300 kHz in order to calibrate for test of components that claim to support both 1.5 Gb/s and 3.0 Gb/s rates.

Observable Results: Record the peak-to-peak frequency deviation of the known modulation divided by the peak-to-peak deviation voltage measured in Hz per Volt for each of the 1.5 GHz and 3.0 GHz measurements as the two calibration factors for 1.5 Gb/s and 3.0 Gb/s tests respectively..

Appendix D:

Calibration of Test Setup Differential Skew.

Purpose: Calibration of the skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can improve the accuracy of the differential skew test in TSG-03.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- One low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: June 1, 2006

Discussion: The skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can directly increase or decrease the measured differential skew of the DUT. This calibration removes the effect of these skews from the test.

Calibration Setup as shown in Appendix B: Except the BERTScope clock output is connected to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Initially connect the BERTScope Data Output + port to the one of the short matched pair of SMA Male to Male Cables that connects to the CR 12500A Data Input + ports.

Calibration Procedure:

1. Use the MFTP pattern, but generated by the pattern generator of the BERTScope Data Output + port. The MFTP pattern is pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern then click "Enable Outputs".
2. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Zoom in on the right most crossing by clicking on it and dragging it to the center of the display.
3. Click on "Eye Setup" on the BERTScope then "Cursors" and select "Time Cursors". Place one cursor at the mid point of the rising edge. Place the second cursor near by and zoom in on the mid point by changing the time and/or voltage scale. It is desirable to allow the time scale to show a full 20 ps to either side of the mid point cursor.
4. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
5. Connect the BERTScope Data Output + port to the CR 12500A Data Input - port via the other short cable that is used between the iSATA receptacle to SMA Female Adapter and the CR 12500A Data Input - port in the setup to be calibrated.
6. Place the second cursor at the mid point of the rising edge. The delta between the first and second cursor is the skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths.

Observable Results: Record the calibrated differential skew for this value to be subtracted from the measured differential skew in TSG-03.

Appendix E:

Fast SATA Testing.

It is recommended to run all tests that require the same DUT pattern in a sequence, then switch pattern and run another sequence of tests in order to expedite and automate testing since the time to initiate DUT in various BIST modes with different patterns take longer time than changing the views on the BERTScope.

To assist the test using sequences the following Table has been provided. For complete test reference one should consult the entire MOI and the following references:

1. Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf
2. Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2i.doc
3. Serial ATA Interoperability Program Policy Document, LogoTF_Policy_v1_0RC2c.doc

SATA Test	#1	#2	#3	#4
PHY-01	HFTP			
PHY-02	HFTP			
PHY-03	HFTP			
PHY-04	HFTP			
TSG-01	HFTP	LBP	MFTP	
TSG-02	HFTP			
TSG-03	HFTP		MFTP	
TSG-04			MFTP	
TSG-05	HFTP		MFTP	
TSG-06	HFTP		MFTP	
TSG-09*	HFTP	LBP		SSOP
TSG-10*	HFTP	LBP		SSOP
TSG-11	HFTP	LBP		SSOP
TSG-12	HFTP	LBP		SSOP

*at 1.5 Gb/s only

It is further convenient to run all LBP tests through TSG-12 then run the SSOP in the opposite order switch to HFTP and run TSG-09 through TSG-12 followed by PHY-01 through PHY-04 and TSG-01 so that one will run all the differential test that do not require switching cables first and eliminates setting up TSG-12 and TSG-09 one additional time each.

Please also note that each of the pairs of measurement results, TSG-01 and TSG-02; TSG-09 and TSG-10; TSG-11 and TSG-12 are obtained with one test per pattern per pair.

SSOP tests are optional and therefore kept for the end time permitting.