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Serial ATA Interoperability Program
Agilent Technologies, Inc. Method of Implementation (MOI) Document for SATA PHY, TSG & OOB Measurements (Real-time DSO Measurements)

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MODIFICATION RECORD

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  Andy Baldman: Initial Release

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  Bryan Kantack: Initial Release

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  Bryan Kantack: Updates made to reflect IW Event #1 Unified Test Document changes

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  Bryan Kantack: Removal of TX/RX test sections, incorporation of first-pass reviewer feedback

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  Bryan Kantack: Update SATA templates to Rev 2.1 for all measurements; OOB timing updates for OOB-01 through OOB-07

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  Bryan Kantack: General formatting and updates to align with Unified Test Document Rev 1.0RC2i (May 11, 2006); added Unified Test Document section references to each measurement

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ACKNOWLEDGMENTS

INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose
The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References
This section specifies all reference material *external* to the test suite, including the specific subclauses references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g., "Appendix 6.A", or "Table 6.1.1-1")

Resource Requirements
The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification
This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

Test Setup
The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section (next).

Procedure
The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or other external sources that may provide more detail regarding these issues.

GROUP 1: PHY GENERAL REQUIREMENTS

Overview:

This group of tests verifies the Phy General Requirements, as defined in Section 2.11 of the Serial ATA Interoperability Unified Test Document, Revision 0.93 (which references the Serial ATA, Revision 2.5).

Test PHY-01 - Unit Interval

Purpose: To verify that the Unit Interval of the DUT TX signaling is within the conformance limits.

References:
        [1] SATA Standard, 7.2.1, Table 20 – General Specifications
        [2] Ibid, 7.2.2.1.3 – Unit Interval
        [3] Ibid, 7.4.11 – SSC Profile
        [4] SATA Interoperability Program Unified Test Document, 2.10.1 – Unit Interval

Resource Requirements:
        Agilent DSO81204A/B (12GHz bandwidth, 40GS/s per channel on 2 channels) with
        Agilent N5411A SATA Electrical Performance Validation and Compliance Test Software
        COMAX iSATA(cable connector) to SMA(f) test fixture distributed by CRUZ Systems (H303000204)
        Gen2i capable host PC running ULink, any other mechanism that makes the device produce the required
patterns is acceptable.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the general PHY conformance limits for SATA devices. This specification includes conformance limits for the mean Unit Interval (UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

        In this test, the mean UI value is measured based on the average of at least 100,000 observed UI's, measured at the transmitter output.

The mean UI is measured from a Unit Interval measurement trend, and applies to signaling with SSC enabled and/or disabled. This value includes the long term frequency accuracy and the Spread Spectrum Clock FM frequency deviation. Tui max and Tui min are also measured.

Test Setup:
        The N5411A automated test software will prompt you to make the device produce HFTP. When prompted, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
        1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
        2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
        3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
        4) In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah.
        5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
        6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is HFTP, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. This is reported as Tui min and Tui max, with the appropriate limits. Either "PASS" or "FAIL" is shown for the unit interval test in the report generated at the completion of the testing. Both Min and Max tests must pass to pass the unit interval test.

Observable Results:

The mean Unit Interval value shall be between 666.4333 ps and 670.2333 ps for 1.5Gb/s devices, and between 333.2167ps and 335.1167ps for 3.0Gb/s devices.

Possible Problems:

Test PHY-02 – Frequency Long Term Stability

Purpose: To verify that the long term frequency stability of the DUT's transmitter is within the conformance limit.

References:
        [1] SATA Standard, 7.2.1, Table 20 – General Specifications
        [2] Ibid, 7.2.2.1.4 – TX Frequency Long Term Stability
        [3] Ibid, 7.4.6 – Long Term Frequency Accuracy
        [4] SATA Interoperability Program Unified Test Document, 2.10.2 – Frequency Long-Term Stability

Resource Requirements:
        Same requirements as for PHY-01

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the general PHY conformance limits for SATA devices. This specification includes conformance limits for the TX Frequency Long Term Stability. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
        Same setup as for PHY-01. There is no setup change for PHY-02.

Test Procedure:
        This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. This is reported as a ppm error value with respect to the nominal data rate. Either "PASS" or "FAIL" is shown for the frequency long-term stability test in the report generated at the completion of the testing. For non-SSC enabled devices, both Min and Max tests must pass to pass the frequency long-term stability test. For SSC enabled devices, only the Max test must pass to pass the frequency long-term stability test.

The measurement for frequency long-term stability records both the min and max unit interval values after the 1.98MHz filter is applied. The ppm deviation is computed from the following operations and the worst case reported for pass/fail:

Max Test: ((Measured Max – Nominal)/Nominal)*1E6 < +350 ppm for pass
Min Test: ((Measured Min – Nominal)/Nominal)* 1E6 < -350 ppm for pass

Observable Results:
        The Frequency Long Term Stability value shall be between +/- 350ppm for both 1.5Gb/s and 3.0Gb/s devices.

Possible Problems:

Test PHY-03 - Spread-Spectrum Modulation Frequency

Purpose: To verify that the Spread Spectrum Modulation Frequency of the DUT's transmitter is within the conformance limits.

References:
> [1] SATA Standard, 7.2.1, Table 20 – General Specifications
> [2] Ibid, 7.2.2.1.5 – Spread-Spectrum Modulation Frequency
> [3] Ibid, 7.4.11 – SSC Profile
> [4] SATA Interoperability Program Unified Test Document, 2.10.3 – Spread-Spectrum Modulation Frequency

Resource Requirements:
> Same requirements as for PHY-01

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
> Reference [1] specifies the general PHY conformance limits for SATA devices. This specification includes conformance limits for the Spread-Spectrum Modulation Frequency. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

> In this test, the Spread-Spectrum Modulation Frequency, f_{SSC}, is measured, based on at least 10 complete SSC cycles.

> Agilent's N5411A automated SATA compliance software will command the DSO81204B to acquire 2.05MSamples of data at 40GSa/s, or 51.25us of data, which is over 1.5 cycles of the slowest allowed SSC profile frequency at a repeating rate of 30kHz. The DSO81204B will then make 10 acquisitions to acquire a minimum of 15 SSC cycles, which provides sufficient data to analyze the Mean SSC frequency and downspread accuracy.

Test Setup:
> Same setup as for PHY-01. There is no setup change for PHY-03, except that a 1.98MHz low-pass filter (LPF) is applied to the Unit Interval trend to intentionally remove high frequency jitter from the SSC measurement. Reference [1] requires that a LPF with a cutoff frequency of 60 times the 30kHz to 33kHz SSC modulation frequency be applied to the Unit Interval trend for the SSC measurement, which yields a LPF cutoff frequency of 1.8MHz to 1.98MHz. Since 33kHz is an acceptable SSC modulation frequency, the 1.98MHz LPF cutoff frequency at -3dB is used for all DUTs.

Test Procedure:
> This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. The Mean frequency is measured at the 50% threshold of the Unit Interval trend and reported. The Mean is cumulative over all 10 acquisitions and the final Mean SSC modulation frequency is reported as the final value. Either "PASS" or "FAIL" is shown for the SSC frequency test in the report generated at the completion of the testing.

Observable Results:
> The Spread-Spectrum Modulation Frequency value shall be between 30 kHz and 33 kHz for both 1.5Gb/s and 3.0Gb/s devices.

Possible Problems:

Test PHY-04 - Spread-Spectrum Modulation Deviation

Purpose: To verify that the Spread-Spectrum Modulation Deviation of the DUT's transmitter is within the conformance limits.

References:
        [1] SATA Standard, 7.2.1, Table 20 – General Specifications
        [2] Ibid, 7.2.2.1.6 – Spread-Spectrum Modulation Deviation
        [3] Ibid, 7.4.11 – SSC Profile
        [4] SATA Interoperability Program Unified Test Document, 2.10.4 – Spread-Spectrum Modulation Deviation

Resource Requirements:
        Same requirements as for PHY-01

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the general PHY conformance limits for SATA devices. This specification includes conformance limits for the Spread-Spectrum Modulation Deviation. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

        In this test, the Spread-Spectrum Modulation Frequency, f_{SSC}, is measured, based on at least 10 complete SSC cycles.

        Agilent's N5411A automated SATA compliance software will command the DSO81204B to acquire 2.05MSamples of data at 40GSa/s, or 51.25us of data, which is over 1.5 cycles of the slowest allowed SSC profile frequency at a repeating rate of 30kHz. The DSO81204B will then make 10 acquisitions to acquire a minimum of 15 SSC cycles, which provides sufficient data to analyze the SSC frequency and downspread accuracy.

        Note that Tui min limit includes 350ppm tolerance above 0ppm and Tui max limit includes 350ppm tolerance below -5000ppm but the modulation deviation calculation does not include those tolerances since a 1.98MHz LPF is being applied to the Unit Interval measurement trend, intentionally excluding high-frequency jitter from the SSC measurement.

Test Setup:
        Same setup as for PHY-01. There is no setup change for PHY-04, except that a 1.98MHz low-pass filter (LPF) is applied to the Unit Interval trend to intentionally remove high frequency jitter from the SSC measurement. Reference [1] requires that a LPF with a cutoff frequency of 60 times the 30kHz to 33kHz SSC modulation frequency be applied to the Unit Interval trend for the SSC measurement, which yields a LPF cutoff frequency of 1.8MHz to 1.98MHz. Since 33kHz is an acceptable SSC modulation frequency, the 1.98MHz LPF cutoff frequency at -3dB is used for all DUTs.

Test Procedure:
        This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. The Min and Max Unit Interval is measured over the entire trend and converted to ppm deviation. The Mean is cumulative over all 10 acquisitions and the final Min and Max SSC modulation deviation reported as the final value. Either "PASS" or "FAIL" is shown for the SSC modulation deviation test in the report generated at the completion of the testing.

The measurement for SSC modulation deviation records both the min and max unit interval values after the 1.98MHz filter is applied. The ppm deviation is computed from the following operations and the worst case reported for pass/fail:

Min Test: ((Measured Min – Nominal)/Nominal)*1E6 < -5000 ppm for pass

Observable Results:
> The Spread-Spectrum Modulation Deviation value shall be above -5000 ppm for both 1.5Gb/s and 3.0Gb/s devices.

Possible Problems:
> We have seen many devices that have less than 5000ppm of modulation deviation (frequency downspread), but that are 'shifted' such that the maximum data rate on the bus (minimum UI) is faster than the allowed ppm deviation. The upper limit of the SSC modulation deviation test is 0ppm, and does not include the +/-350ppm limits allowed for long-term stability over the entire modulation frequency range of the active link. Comparison tests have been conducted between the oscilloscope measurement trend method and a spectrum analyzer to determine the differences observed between the two measurement methods. Generally, spectrum analyzers will have additional sideband information that is ignored in traditional readings, and may report lower ppm deviation tolerances than the oscilloscope filtered Unit Interval trend method. The example SSC test from an Agilent DSO81204B below shows a device with a Data Rate (inverse of Unit Interval) that is +616ppm fast per the specification. An Agilent 8565E 50GHz spectrum analyzer with a RBW of 10kHz, sweep rate of 8 seconds and span of 15MHz reported +100ppm on the same DUT.
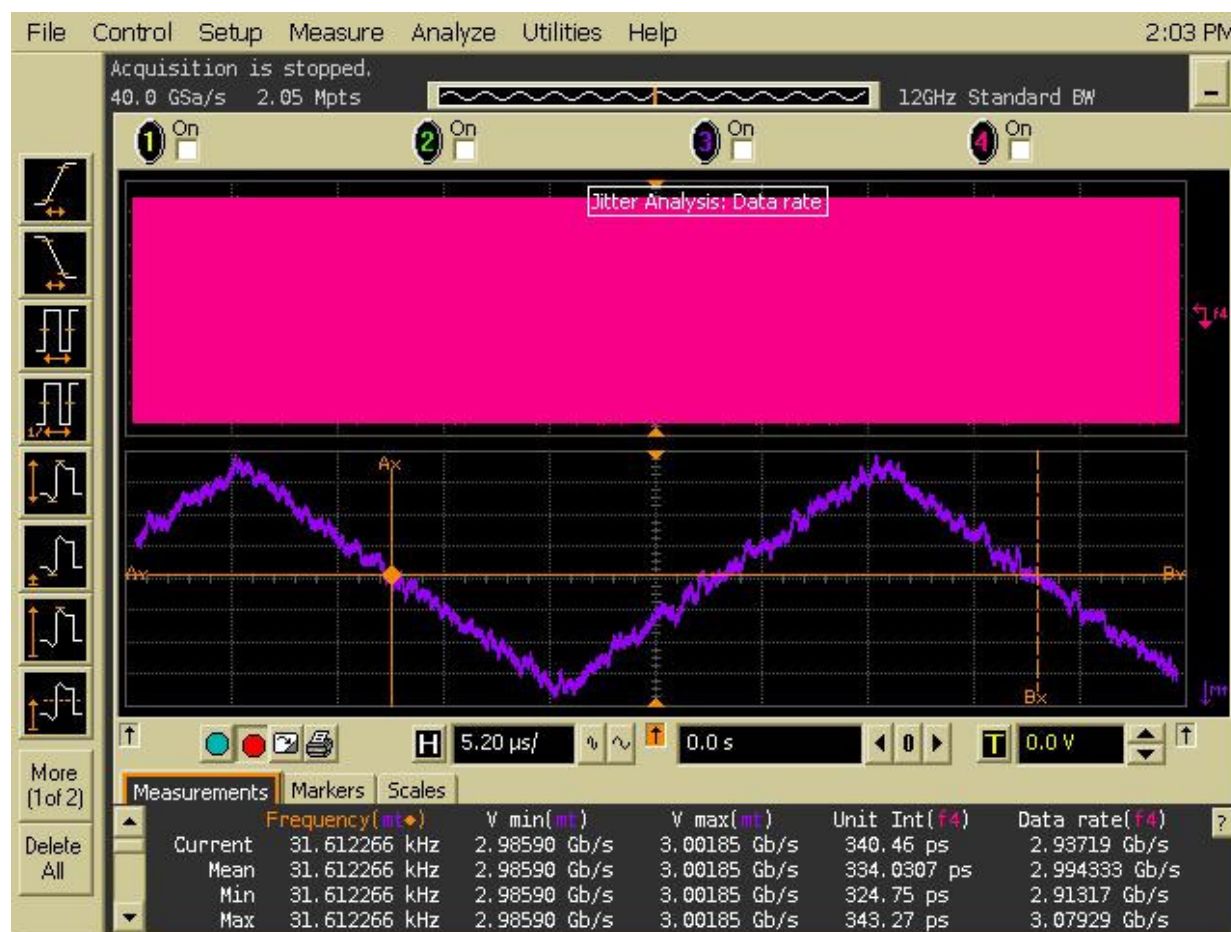
GROUP 2: PHY TRANSMITTED SIGNAL REQUIREMENTS

Overview:

  This group of tests verifies the Phy Transmitted Signal Requirements, as defined in Section 2.13 of the SATA Interoperability Unified Test Document, v0.9 (which references the SATA Standard, v2.5).

Test TSG-01 - Differential Output Voltage

Purpose: To verify that the Differential Output Voltage of the DUT's transmitter is within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.1 – TX Differential Output Voltage
[3] Ibid, 7.4.4 – Transmitter Amplitude
[4] SATA Interoperability Program Unified Test Document, 2.12.1 – Differential Output Voltage

Resource Requirements:
Same as for PHY-01, repeated here for convenience:
Agilent DSO81204A/B (12GHz bandwidth, 40GS/s per channel on 2 channels) with
Agilent N5411A SATA Electrical Performance Validation and Compliance Test Software
COMAX iSATA(cable connector) to SMA(f) test fixture distributed by CRUZ Systems (H303000204)
Gen2i capable host PC running ULink, any other mechanism that makes the device produce the required patterns is acceptable.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the Differential Output Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Vdiff Min is tested with HFTP, MFTP and LBP. Vdiff Max is tested with MFTP and LFTP.

Note that LBP depends on the Running Disparity, which cannot be known. See possible problems, below.

Test Setup:
Since PHY-01 the device has been producing HFTP and it is already connected to the scope. The N5411A SATA compliance software will prompt for MFTP and LFTP when it needs those patterns. When prompted for MFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) In the User Patterns combo box, choose the User Patterns selection. Now enter 78787878h 78787878h into the 64-bit Data (Hex) boxes just above the User Patterns combo box. This will encode as a repeating D24.3 on the line and provide a half-rate clock-like data pattern (1100110011).
5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

When prompted for LBP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:

1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) In the User Patterns combo box, choose the Lone-Bit Pattern (+ve) selection. This is implemented as 8BFC8DFCh 8EFC8BFCh.
5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is LBP, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Interim values for UH (HFTP upper), LH (HFTP lower), UM (MFTP upper), LM (MFTP lower), DHM (worst-case differential HFTP or differential MFTP), A (LBP lone 1-bit upper) and B (LBP lone 0-bit lower) are measured and computed to determine the final Vtest value for the Minimum Amplitude test. These interim values and screen captures can also be a helpful aid in debugging which pattern, and specifically, which bit failed the test. Similar steps are used to setup the MFTP and LFTP patterns used for the Maximum Amplitude test.

NOTE: The N5411A maximum amplitude test does not test physical voltage, but instead, the ratio of amplitude histogram points at or above the physical specification limit compared to total amplitude histogram points at or above +/- DOV/2. Again, pu, nu, NU, pl, nl and NL are reported out to assist in debug. This methodology is provided per the VdiffTX, Max measurement definition in reference [1]. Either "PASS" or "FAIL" is shown for the minimum amplitude test in the report generated at the completion of the testing.

Reference [4] addresses the measurement of VdiffTX, Min and VdiffTX, Max per the SATA-IO LOGO IW testing requirements as follows:

DOV Min = Vtest(min) = min(DH, DM, VtestLBP)
DOV Max = Vtest(max) = max(DH, DM, VtestLBP)

Observable Results:

The Differential Output Voltage shall be between the limits specified in reference [4]. For convenience, the values are reproduced below. For the differential amplitude voltage test to pass, the following two conditions must both be met: 1) The minimum differential amplitude value, Vtest(min), must meet the DOV minimum test limits, 2) the maximum differential amplitude value, Vtest(max), must meet the DOV maximum test limits.

Device Type	DOV Min	DOV Max
Gen1i	400 mV	800 mV
Gen2i	400 mV	800 mV

Possible Problems:

The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-02 - Rise/Fall Time

Purpose: To verify that the Rise/Fall time of the DUT's transmitter is within the conformance limits.

References:
> [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
> [2] Ibid, 7.2.2.3.3 – TX Rise/Fall Time
> [3] Ibid, 7.4.3 – Rise and Fall Times
> [4] SATA Interoperability Program Unified Test Document, 2.12.2 – Rise/Fall Time

Resource Requirements:
> Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
> Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the Rise/Fall Time. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

> TSG-02 is tested using HFTP.

> The cables connecting the COMAX SATA TEST FIXTURE DISTRIBUTED BY CRUZ SYSTEMS (H303000204) to the scope must be deskewed, as discussed in Appendix A. Skew lengthens the measured differential rise and fall times.

Test Setup:
> The N5411A SATA compliance software will prompt for HFTP when it needs that patterns. When prompted for HFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
> 1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
> 2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
> 3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
> 4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah.
> 5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
> 6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:
> This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. The Min, Max and Mean Rise and Fall Times are measured over the entire data

acquisition (about 38,000 rising and 38,000 falling edges per acquisition). The Mean value is reported as the final value and compared only to the RFT Max value in the table below for pass/fail. Either "PASS" or "FAIL" is shown for the Rise/Fall time test in the report generated at the completion of the testing.

Observable Results:

The Mean TX Rise/Fall Times shall be between the limits specified in reference [1]. For convenience, the values are reproduced below. Note: Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interoperability testing.

Device Type	RFT Min	RFT Max
Gen1i	100 ps	273 ps
Gen2i	67 ps	136 ps

Possible Problems:

Test TSG-03 - Differential Skew

Purpose: To verify that the Differential Skew of the DUT's transmitter is within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.4 – TX Differential Skew (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.12 – Intra-pair Skew
[4] SATA Interoperability Program Unified Test Document, 2.12.3 – Differential Skew

Resource Requirements:
Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for Differential Skew. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Skew is measured with HFTP and MFTP.

The cables connecting the COMAX SATA TEST FIXTURE DISTRIBUTED BY CRUZ SYSTEMS (H303000204) to the scope must be deskewed, as discussed in Appendix A. Uncompensated cable skew contributes directly to measured differential skew.

Test Setup:
The N5411A SATA compliance software will prompt for HFTP and MFTP when it needs those patterns. When prompted for HFTP or MFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. For MFTP: In the User Patterns combo box, choose the User Patterns selection. Now enter 78787878h 78787878h into the 64-bit Data (Hex) boxes just above the User Patterns combo box. This will encode as a repeating D24.3 on the line and provide a half-rate clock-like data pattern (1100110011).
5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Differential skew is measured as the difference between the mean of the rising edge in a single-ended eye diagrams of TX+ and the mean of the falling edge in a single-ended eye diagram of TX–, repeat the measurement this time measuring the difference between the mean of the rising edge in a single-ended eye diagrams of TX- and the mean of the falling edge in a single-ended eye diagram of TX+, finally compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement in accordance with section 7.4.12 of the Serial ATA revision 2.5. Two differential skew values are provided, one for HFTP and one for MFTP, and both must meet the Max Diff Skew requirements in reference [1], which are repeated in the table below for convenience. Either "PASS" or "FAIL" is shown for the differential skew test in the report generated at the completion of the testing.

Observable Results:
        The TX Differential Skew shall be between the limits specified in reference [1]. For convenience, the values are reproduced below.

Device Type	Max Diff Skew
Gen1i	20 ps
Gen2i	20 ps

Possible Problems:

Test TSG-04 - AC Common Mode Voltage

Purpose: To verify that the AC Common Mode Voltage of the DUT's transmitter is within the conformance limits.

References:
        [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
        [2] Ibid, 7.2.2.3.5 – TX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)
        [3] Ibid, 7.4.17 – TX AC Common Mode Voltage
        [4] SATA Interoperability Program Unified Test Document, 2.12.4 – AC Common Mode Voltage

Resource Requirements:
        Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TX AC Common Mode Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

        TSG-04 is tested with MFTP.

        The cables connecting the COMAX SATA TEST FIXTURE DISTRIBUTED BY CRUZ SYSTEMS (H303000204) to the scope must be deskewed, as discussed in Appendix A. Skew contributes directly to common mode spikes which if large enough, even though they are low pass filtered to half the bit rate, can cause failure.

Test Setup:
        The N5411A SATA compliance software will prompt for MFTP. When prompted for MFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) In the User Patterns combo box, choose the User Patterns selection. Now enter 78787878h 78787878h into the 64-bit Data (Hex) boxes just above the User Patterns combo box. This will encode as a repeating D24.3 on the line and provide a half-rate clock-like data pattern (1100110011).
5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. The test is performed as (TX+ + TX-)/2, low-pass filter applied with a -3dB cutoff frequency of bit-rate/2 and peak-peak amplitude of the filter output measured as the final AC common mode voltage value. Either "PASS" or "FAIL" is shown for the common mode voltage test in the report generated at the completion of the testing.

Observable Results:
The AC Common Mode Voltage value shall be less than 50 mVp-p for Gen2i and Gen2m devices.

Possible Problems:

Test TSG-05 - Rise/Fall Imbalance

Purpose: To verify that the Rise/Fall Imbalance of the DUT's transmitter is within the conformance limits.

References:
        [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
        [2] Ibid, 7.2.2.3.9 – TX Rise/Fall Imbalance
        [3] Ibid, 7.4.16 – TX Rise/Fall Imbalance
        [4] SATA Interoperability Program Unified Test Document, 2.12.5 – Rise/Fall Imbalance

Resource Requirements:
        Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the Rise/Fall Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

        Rise/Fall imbalance is measured with HFTP and MFTP. References [2] and [3] both define two values to be computed, for each pattern. The two values compare TX+ rise to TX- fall, and TX- rise to TX+ fall. The results are expressed as a percentage of the average of the two items being compared.

Test Setup:
        The N5411A SATA compliance software will prompt for HFTP and MFTP when it needs those patterns. When prompted for HFTP or MFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
        1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
        2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
        3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
        4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. For MFTP: In the User Patterns combo box, choose the User Patterns selection. Now enter 78787878h 78787878h into the 64-bit Data (Hex) boxes just above the User Patterns combo box. This will encode as a repeating D24.3 on the line and provide a half-rate clock-like data pattern (1100110011).
        5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
        6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the rise/fall imbalance test in the report generated at the completion of the testing.

Observable Results:

The Rise/Fall Imbalance value shall be less than 20% for Gen2i and Gen2m devices.

Possible Problems:

Test TSG-06 - Amplitude Imbalance

Purpose: To verify that the Amplitude Imbalance of the DUT's transmitter is within the conformance limits.

References:
> [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
> [2] Ibid, 7.2.2.3.10 – TX Amplitude Imbalance (Gen2i, Gen1x, Gen2x)
> [3] Ibid, 7.4.15 – TX Amplitude Imbalance
> [4] SATA Interoperability Program Unified Test Document, 2.12.6 – Amplitude Imbalance

Resource Requirements:
> Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
> Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TX Amplitude Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

> Amplitude Imbalance is measured with HFTP and MFTP.

> This parameter is a measure of the match in the single-ended amplitudes of the TX+ and TXsignals. The test setup shown Figure 109 shall be used for this measurement. This parameter shall be measured and met with both the HFTP and MFTP patterns. Clock-like patterns are used here to enable the use of standard mode-based amplitude measurements for the sole purpose of determining imbalance. The measurement of differential amplitude uses a different method. In order to determine the amplitude imbalance, single ended mode high and mode low based amplitudes of both TX+ and TX- over 10 to 20 cycles of the clock-like pattern being used shall be determined. The amplitude imbalance value for that pattern is then determined by the equation:

absolute value(TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2

Test Setup:
> The N5411A SATA compliance software will prompt for HFTP and MFTP when it needs those patterns. When prompted for HFTP or MFTP, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
> 1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
> 2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
> 3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
> 4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. For MFTP: In the User Patterns combo box, choose the User Patterns selection. Now enter 78787878h 78787878h into the 64-bit Data (Hex) boxes just above the User Patterns combo box. This will encode as a repeating D24.3 on the line and provide a half-rate clock-like data pattern (1100110011).
> 5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
> 6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables

(Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the rise/fall imbalance test in the report generated at the completion of the testing.

Observable Results:

The TX Amplitude Imbalance value shall be less than 10% for Gen1x, Gen2i, Gen2m, and Gen2x devices.

Possible Problems:

Test TSG-07 - TJ at Connector, Data, 5UI

Purpose: To verify that the TJ at Connector (Data, 5UI) of the DUT's transmitter is within the conformance limits.

References:
> [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
> [2] Ibid, 7.2.2.3.11
> [3] Ibid, 7.4.8
> [4] SATA Interoperability Program Unified Test Document, 2.12.7 – TJ at Connector, Data, 5UI

Resource Requirements:
> Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
> Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TJ at Connector (Data, 5UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

> As noted directly in Reference [4], this test is **OPTIONAL** for all components. For components which support 3Gb/s, this requirement would be tested at 1.5Gb/s. For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

> For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
> The N5411A SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
> 1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
> 2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
> 3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
> 4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
> 5) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:
> This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the TJ at Connector, Data, 5UI test in the report generated at the completion of the testing.

Observable Results:

The TJ at Connector (Data, 5UI) value shall be less than 0.355 UI for Gen1i and Gen1m devices.

Possible Problems:

The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-08 - DJ at Connector, Data, 5UI

Purpose: To verify that the DJ at Connector (Data, 5UI) of the DUT's transmitter is within the conformance limits.

References:
>   [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
>   [2] Ibid, 7.2.2.3.11
>   [3] Ibid, 7.4.8
>   [4] SATA Interoperability Program Unified Test Document, 2.12.8 – DJ at Connector, Data, 5UI

Resource Requirements:
>   Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the DJ at Connector (Data, 5UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

As noted directly in Reference [4], this test is **OPTIONAL** for all components. For components which support 3Gb/s, this requirement would be tested at 1.5Gb/s. For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
The N5411A SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
5) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the DJ at Connector, Data, 5UI test in the report generated at the completion of the testing.

Observable Results:

The DJ at Connector (Data, 5UI) value shall be less than 0.175 UI for Gen1i and Gen1m devices.

Possible Problems:

The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-09 - TJ at Connector, Data, 250UI

Purpose: To verify that the TJ at Connector (Data, 250UI) of the DUT's transmitter is within the conformance limits.

References:
>   [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
>   [2] Ibid, 7.2.2.3.11
>   [3] Ibid, 7.4.8
>   [4] SATA Interoperability Program Unified Test Document, 2.12.9 – TJ at Connector, Data, 250UI

Resource Requirements:
>   Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
>   Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TJ at Connector (Data, 250UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

>   As noted directly in Reference [4], for components which support 3Gb/s, this requirement would be tested at 1.5Gb/s. For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. Specifically, a second-order PLL with a loop bandwidth of (data rate / 500) and a damping factor of 0.707 is used to perform the clock recovery for measuring the time interval error prior to the jitter separation being performed. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

>   For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
>   The N5411A SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
>   6) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
>   7) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
>   8) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
>   9) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
>   10) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the TJ at Connector, Data, 250UI test in the report generated at the completion of the testing.

Observable Results:
 The TJ at Connector (Data, 250UI) value shall be less than 0.47 UI for Gen1i and Gen1m devices.

Possible Problems:
 The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-10 - DJ at Connector, Data, 250UI

Purpose: To verify that the DJ at Connector (Data, 250UI) of the DUT's transmitter is within the conformance limits.

References:
       [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
       [2] Ibid, 7.2.2.3.11
       [3] Ibid, 7.4.8
       [4] SATA Interoperability Program Unified Test Document, 2.12.01 – DJ at Connector, Data, 250UI

Resource Requirements:
       Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
       Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the DJ at Connector (Data, 250UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

       As noted directly in Reference [4], for components which support 3Gb/s, this requirement would be tested at 1.5Gb/s. For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. Specifically, a second-order PLL with a loop bandwidth of (data rate / 500) and a damping factor of 0.707 is used to perform the clock recovery for measuring the time interval error prior to the jitter separation being performed.   In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

       For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
       The N5411A SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
       11) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
       12) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
       13) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
       14) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
       15) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the DJ at Connector, Data, 250UI test in the report generated at the completion of the testing.

Observable Results:
>   The DJ at Connector (Data, 250UI) value shall be less than 0.22 UI for Gen1i and Gen1m devices.

Possible Problems:
>   The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-11 - TJ at Connector, Clock, 500

Purpose: To verify that the TJ at Connector (Clock, 500) of the DUT's transmitter is within the conformance limits.

References:
  [1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
  [2] Ibid, 7.2.2.3.12
  [3] Ibid, 7.4.6, 7.4.8
  [4] SATA Interoperability Program Unified Test Document, 2.12.11 – TJ at Connector, Clock, 500

Resource Requirements:
  Same as for TSG-01

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
  Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TJ at Connector (Clock, 500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

  This test applies to Gen2i (3.0Gbps) devices. Since estimating TJ at a BER of 10^-12 requires first separating DJ from the higher error probability CDF, TSG-11 and TSG-12 results are measured at the same time.

  For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
  The N5411A SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted for these patterns, if you will use the ULink DriveMaster 2006 software to put the device into BIST, follow this procedure:
1) Connect a SATA cable from the host system's port 0 SATA connection to the device under test.
2) Launch DriveMaster 2006 on the host system and choose the 'Ctl SATA' Control Panel icon from DriveMaster's menu bar. The default SATA Phy Control port is port 0.
3) From the BIST method combo box, choose the appropriate supported BIST method for communicating with the drive. For the 80-bit Transmit only test option with ALIGN bypass and scramble bypass, choose T+S+A; for the far-end retimed loopback mode, choose L.
4) For HFTP: In the User Patterns combo box, choose the High-Transition Density Pattern (HTDP). This is implemented as the HFTP, or 4A4A4A4Ah 4A4A4A4Ah. For LBP: In the User Patterns combo box, choose the Lone-Bit Pattern (+ve) selection. This is implemented as 8BFC8DFCh 8EFC8BFCh. For SSOP: In the User Patterns combo box, choose the SSOP selection. This is implemented as 7F7F7F7Fh 7F7F7F7Fh.
5) Click the 'BIST' button to initiate the BIST command script, and wait for the status in the lower left-hand corner of the SATA Control Panel dialog to update to BIST FIS SUCCEEDED. If the status reads BIST FIS FAILED, click the COMRESET radio button and repeat steps 3-5.
6) Disconnect the SATA cable from the device and plug in the H303000204 test fixture. The H303000204 is connected to channels 1 and 3 of the DSO81204A/B by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411A prompt. If not, the device did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:
The TJ shall be less than 0.37UI when measured at f_{BAUD}/500 for 3.0GB/s devices.

Possible Problems:
The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

Test TSG-12 - DJ at Connector, Clock, 500

Purpose: To verify that the DJ at Connector (Clock, 500) of the DUT's transmitter is within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.12
[3] Ibid, 7.4.6, 7.4.8
[4] SATA Interoperability Program Unified Test Document, 2.12.12 – DJ at Connector, Clock, 500

Resource Requirements:
Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the DJ at Connector (Clock, 500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

This test applies to Gen2i (3.0Gbps) devices. Since estimating TJ at a BER of 10^-12 requires first separating DJ from the higher error probability CDF, TSG-11 and TSG-12 results are measured at the same time.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and if time permits should also be made with SSOP.

Test Setup:
This test result is derived at the same time as TSG-11. Therefore, no setup change is needed for TSG-12.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:
The DJ shall be less than 0.19UI when measured at f_{BAUD}/500 for 3.0GB/s devices.

Possible Problems:
The SATA specification includes a pattern that makes LBP for RD+, and another if RD-. Since RD is not known, with either one there is a 50% chance that LBP will actually be produced correctly on the line. ULink's DriveMaster program provides both +ve and –ve versions of the LBP to ensure that this test can be performed correctly per the specification. The Agilent N5411A SATA compliance software will wait for the scope to trigger on and identify the 4-1-3 lone-bit pattern prior to performing the test. If the lone-bit cannot be identified, the N5411A will prompt you to try a different pattern. Return to the Test Setup section of this measurement and repeat steps 4 and 5, using the Lone-Bit Pattern (-ve) selection in the ULink DriveMaster software instead. After 2-3 BIST enable attempts with each pattern, you should be able to complete the Minimum Amplitude test. If not, a non-standard way to enable the Lone-Bit Pattern will be required.

GROUP 3: PHY OOB REQUIREMENTS

Overview:

This group of tests verifies the Phy OOB Requirements, as defined in Section 2.15 of the SATA Interoperability Unified Test Document, v0.9 (which references the SATA Standard, v2.5).

Test OOB-01 – OOB Signal Detection Threshold

Purpose: To verify that the OOB Signal Detection Threshold of the DUT's receiver is within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
[2] Ibid, 7.2.2.7.1
[3] Ibid, 7.4.20
[4] SATA Interoperability Program Unified Test Document, 2.14.1 – OOB Signal Detection Threshold

Resource Requirements:
Agilent DSO81204A/B (12GHz bandwidth, 40GS/s per channel on 2 channels) with
Agilent N5411A SATA Electrical Performance Validation and Compliance Test Software
COMAX iSATA(cable connector) to SMA(f) test fixture distributed by CRUZ Systems (H303000204)
Agilent 81134A 2-channel 3.35GHz Pulse/Pattern Generator
Agilent 33340C 20dB DC-26.5GHz Passive Attenuator (Qty. 2 needed)
Agilent 11636B Power Divider (not power splitter) DC-26.5GHz (Qty. 2 needed)
Agilent 5062-6681 6-inch SMA cable (Qty. 4 needed to mix 81134A outputs for OOB testing)
Agilent 1169A 13GHz Differential Active Voltage Probe with
    N5381A 13GHz Differential Solder-In Probe Head (to verify differential amplitude of signal delivered to the differential RX input on the device under test and monitor the Device TX Output response) (Qty. 2 needed)

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the OOB Signal Detection Threshold. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

This test is done by attenuating the output of the 81134A differential pair that is connected to the DUT's RX input pair through the CRUZ SYSTEMS' H303000204 test fixture in incremental steps to determine the point at which the device state machine fails to consistently respond to the input data from the 81134A. This test can easily be performed using the BIST-L far-end digital retimed loopback mode and a fixed test pattern. The next best alternative is to have the 81134A continuously issue a nominal OOB COMRESET and COMWAKE burst sequence and to monitor the device COMINIT and COMWAKE response, and to observe when the device COMWAKE response ceases to exist. Because the 81134A can adjust signal amplitudes in 1mV increments down to 50mV, the lower limits of the OOB Signal Detection Threshold can be accurately measured using the mixed 81134A output shown in the image following the Test Setup section of this measurement definition. Should you desire to test the OOB detection threshold to lower than 50mV, a single 20dB passive attenuator can be added to each of the 81134A mixed outputs, allowing you to test from 200mV down to 5mV. The 81134A offers amplitude control from its Channel menu. In order to make the most accurate measurement of voltage of the OOB stimulus being applied to the device under test's RX input, a high-impedance active voltage probe with at least 12GHz of bandwidth should be used to measure the voltage directly at the mated connector pair during this test

Test Setup:
The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is

running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation. The following setup diagram, provided in the Agilent N5411A SATA test software prior to running the OOB tests, will guide the correct connection of the 11636B Power Dividers to the inputs of the 81134A Pattern Generator using the 5062-6681 short SMA cables. This allows for the electrical idle to be properly generated by the pattern generator prior to sending the OOB signals to the device under test. Most pattern generators cannot generate a tri-state signal with proper electrical idle, and power dividers must be used to create these tri-level signals from two channels of a dual-state pattern generator output. More information on this procedure can be found in Annex A. In order to maintain the proper differential polarity and pattern disparity, it is important to ensure that the Channel 1 positive (+) output of the 81134A is mixed with the Channel 2 negative (-) output of the 81134A, as shown in the following diagram, to provide the TX+ signal that will be delivered to the RX+ input on the device under test. The remaining 81134A data outputs, Channel 1 negative (-) and Channel 2 positive (+) are mixed together and delivered to the RX- input on the device under test through the COMAX H303000204 iSATA test fixture.
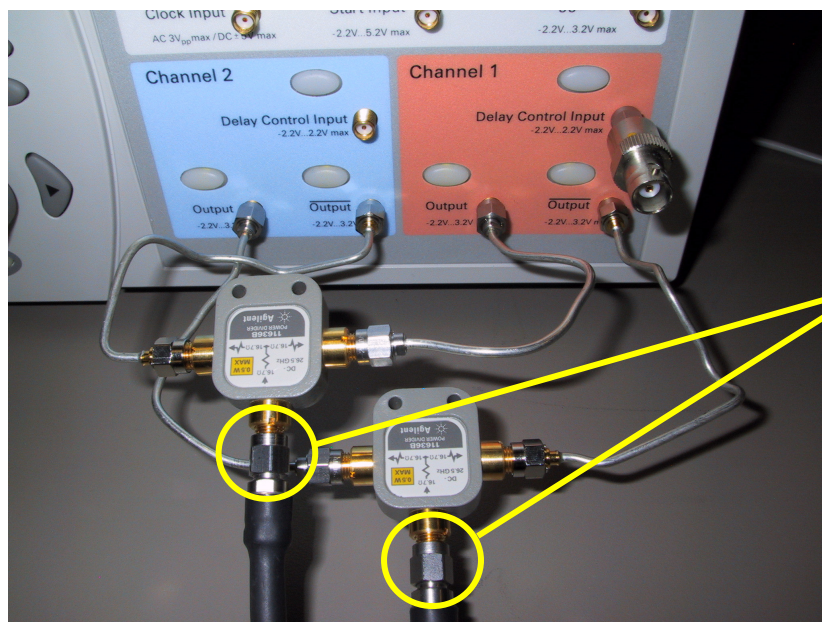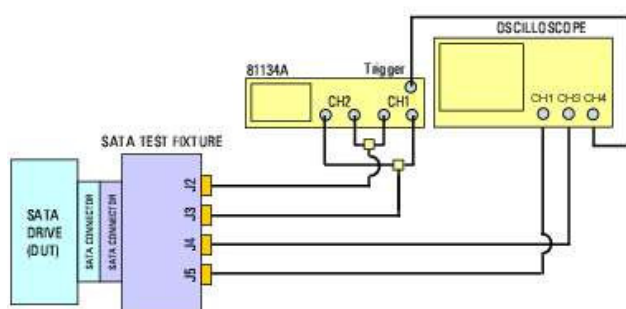
If less than 50mV of differential OOB amplitude is needed at the device receiver, then insert the 33340C 20dB passive attenuators here, one on each of the 11636B power divider outputs, before the SMA cable is attached. The voltage output of the 81134A after the attenuator is now 10 times lower than the voltage selection on the 81134A output. The sensitivity of the adjustment is now 0.1mV instead of 1mV with the divide by 10 attenuator in place.
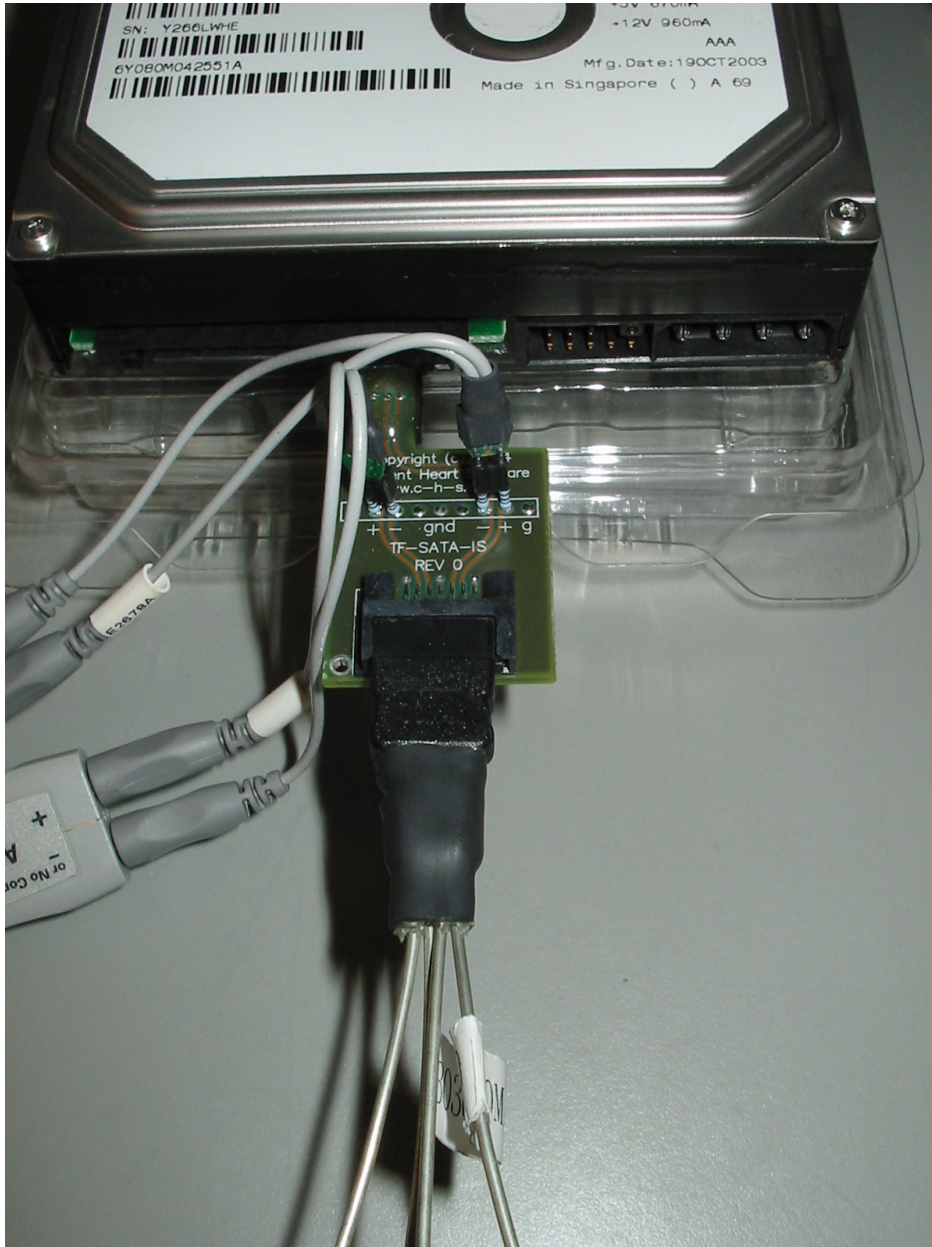
Example Connection: Using a Crescent Heart TF-SATA-IS fixture to accommodate probe attachment on the TX/RX lines without disrupting the signaling between the HOST and Device under test.

Test Procedure:

This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the OOB Signal Detection Threshold test in the report generated at the completion of the testing.

To execute this test on a device which supports 1.5Gb/s, an OOB burst is issued to the device at the following voltage threshold limits:

- 40mV (at this limit, the device is expected to **NOT DETECT** the OOB signaling)
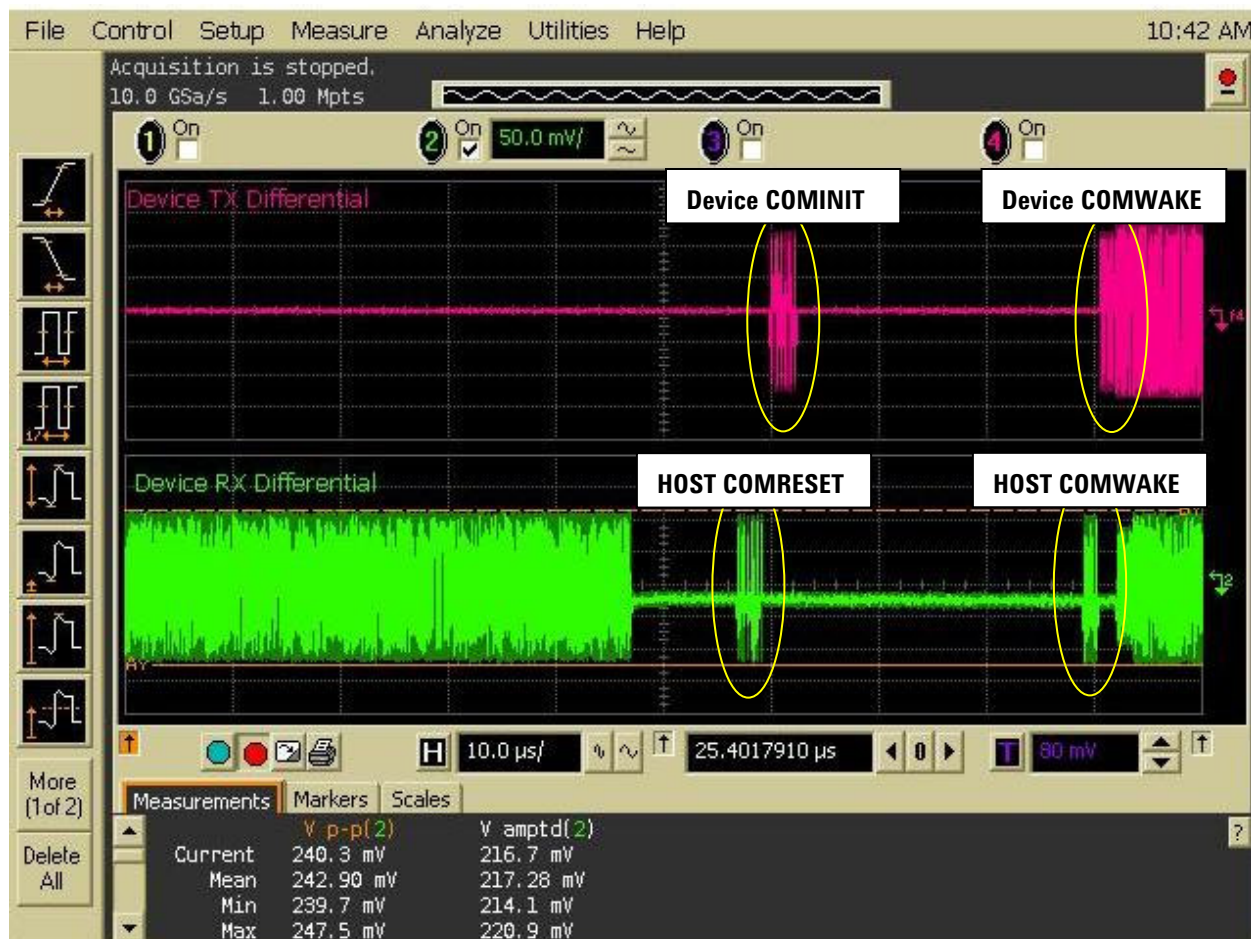- 210mV (at this limit, the device is expected to **DETECT** the OOB signaling)

To execute this test on a device which supports 3Gb/s, an OOB burst is issued to the device at the following voltage threshold limits:

- 60mV (at this limit, the device is expected to **NOT DETECT** the OOB signaling)
- 210mV (at this limit, the device is expected to **DETECT** the OOB signaling)

In this figure, the device correctly responds to a valid in-spec COMRESET/COMWAKE OOB initialization sequence at 210mV, thus passing the threshold test. The other requirement for passing is to successfully REJECT the same HOST OOB signal sent at 40mV (for Gen 1i) or 60mV (for Gen 2i).

Observable Results:
> The OOB Signal Detection Threshold value shall be between 50 and 200 mVp-p for 1.5Gb/s devices.
> The OOB Signal Detection Threshold value shall be between 75 and 200 mVp-p for 3.0Gb/s devices.

Pass/Fail Criteria
- For devices running at 1.5Gb/s:
  - Verification of **NO** device OOB detection at 40mV
  - Verification of device OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the device.
- For devices running at 3Gb/s:
  - Verification of **NO** device OOB detection at 60mV
  - Verification of device OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the device.

Possible Problems:
      Some devices have an active calibration and training routine for timing that may run during the device initialization routine (i.e. during COMWAKE) that may cause a temporary active termination impedance increase that will simultaneously decrease the amplitude of the COMWAKE burst delivered to the device receiver. Please ensure that you send a valid COMRESET to the device at least once after power-on to be sure this calibration routine is completed prior to attempting the OOB Threshold Detection test, as it could cause a false failure on devices with this type of calibration routine.

Test OOB-02 – UI During OOB Signaling

Purpose: To verify that the UI During OOB Signaling of the DUT's transmitter is within the conformance limits.

References:
      [1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
      [2] Ibid, 7.2.2.7.2
      [3] Ibid, 7.4.11
      [4] SATA Interoperability Program Unified Test Document, 2.14.2 – UI During OOB Signaling

Resource Requirements:
      Agilent DSO81204A/B (12GHz bandwidth, 40GS/s per channel on 2 channels) with
      Agilent N5411A SATA Electrical Performance Validation and Compliance Test Software
      COMAX iSATA(cable connector) to SMA(f) test fixture distributed by CRUZ Systems (H303000204)
      Agilent 81134A 2-channel 3.35GHz Pulse/Pattern Generator
      Agilent 33340C 20dB DC-26.5GHz Passive Attenuator (Qty. 2 needed)
      Agilent 11636B Power Divider (not power splitter) DC-26.5GHz (Qty. 2 needed)
      Agilent 5062-6681 6-inch SMA cable (Qty. 4 needed to mix 81134A outputs for OOB testing)

See Appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
      Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the UI During OOB Signaling. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
      The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
      This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the UI During OOB Signaling test in the report generated at the completion of the testing.

Observable Results:
      The UI During OOB Signaling value shall be between 646.67 and 686.67ps.

Possible Problems:

Test OOB-03 – COMINIT/RESET and COMWAKE Transmit Burst Length

Purpose: To verify that the COMINIT/RESET and COMWAKE Transmit Burst Length of the DUT's transmitter is within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
[2] Ibid, 7.2.2.7.3
[3] Ibid, 7.4.21
[4] SATA Interoperability Program Unified Test Document, 2.14.3 – COMINIT/RESET and COMWAKE Transmit Burst Length

Resource Requirements:
Same as for OOB-02.

See appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the COMINIT/RESET and COMWAKE Transmit Burst Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the device COMINIT and COMWAKE Transmit Burst Length test in the report generated at the completion of the testing.

Observable Results:
The device COMINIT and COMWAKE Transmit Burst Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 160. Numerically, the COMINIT and COMWAKE burst lengths should be between 103.47 ns and 109.87 ns, which is 160 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively.

Possible Problems:

Test OOB-04 – COMINIT/RESET Transmit Gap Length

Purpose: To verify that the COMINIT/RESET Transmit Gap Length of the DUT's transmitter is within the conformance limits.

References:
    [1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
    [2] Ibid, 7.2.2.7.4
    [3] Ibid, 7.4.21
    [4] SATA Interoperability Program Unified Test Document, 2.14.4 – COMINIT/RESET Transmit Gap Length

Resource Requirements:
    Same as for OOB-02.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the COMINIT/RESET Transmit Gap Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the device COMINIT/RESET Transmit Gap Length test in the report generated at the completion of the testing.

Observable Results:
The COMINIT/RESET Transmit Gap Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 480. Numerically, the COMINIT and COMRESET gap lengths should be between 310.40 ns and 329.60 ns, which is 480 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively.

✓ COMINIT Inter-burst Timing

Reference: Serial ATA : High Speed Serialized AT Attachment Release 1.0, Section 5.2.2.1

Test Summary: Pass   Test Description: Send in-spec nominal COMRESET to Drive. Verify Drive responds with 6 bursts of COMINIT signal with appropriate inter-burst timing.

Test Limits: 304.00ns <= VALUE <= 336.00ns   Drive : COMInit Interburst Timing   319.77ns

Result Details:

Gap 1 319.73ns   Gap 2 319.77ns   Gap 3 319.73ns   Gap 4 319.73ns   Gap 5 319.69ns

Figure: Drive : COMInit Interburst Timing

Jitter Analysis

Scales
Source   Vertical(V/div)   Offset(V)   Horizontal(s/div)   Position(s)
Function 4 88.50m   -550.0µ   300.0n   4.440µ

✓ Drive COMWAKE Inter-burst Timing

Reference: Serial ATA : High Speed Serialized AT Attachment Release 1.0, Section 5.2.2.2

Test Summary: Pass   Test Description: Send in-spec nominal COMWAKE to Drive. Verify Drive responds with 6 bursts of COMWAKE signal with appropriate inter-burst timing.

Test Limits: 101.30ns <= VALUE <= 112.00ns   Drive : COMWake Interburst Timing   106.42ns

Result Details:

Gap 1 106.42ns   Gap 2 106.38ns   Gap 3 106.39ns   Gap 4 106.36ns   Gap 5 106.42ns

Figure: Drive : COMWake Interburst Timing

Scales
Source   Vertical(V/div)   Offset(V)   Horizontal(s/div)   Position(s)
Function 4 88.50m   -550.0µ   150.0n   8.305µ

Example N5411A OOB Output Report: This is a section of the HTML output report that illustrates and quantifies the COMINIT and COMWAKE Transmit Gap Lengths.

Possible Problems:

Test OOB-05 – COMWAKE Transmit Gap Length

Purpose: To verify that the COMWAKE Transmit Gap Length of the DUT's transmitter is within the conformance limits.

References:
>   [1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
>   [2] Ibid, 7.2.2.7.5
>   [3] Ibid, 7.4.21
>   [4] SATA Interoperability Program Unified Test Document, 2.14.5 – COMWAKE Transmit Gap Length

Resource Requirements:
>   Same as for OOB-02.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
>   Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the COMWAKE Transmit Gap Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
>   The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the device COMWAKE Transmit Gap Length test in the report generated at the completion of the testing.

Observable Results:
>   The COMWAKE Transmit Gap Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 160. Numerically, the COMWAKE gap lengths should be between 103.47 ns and 109.87 ns, which is 160 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively.
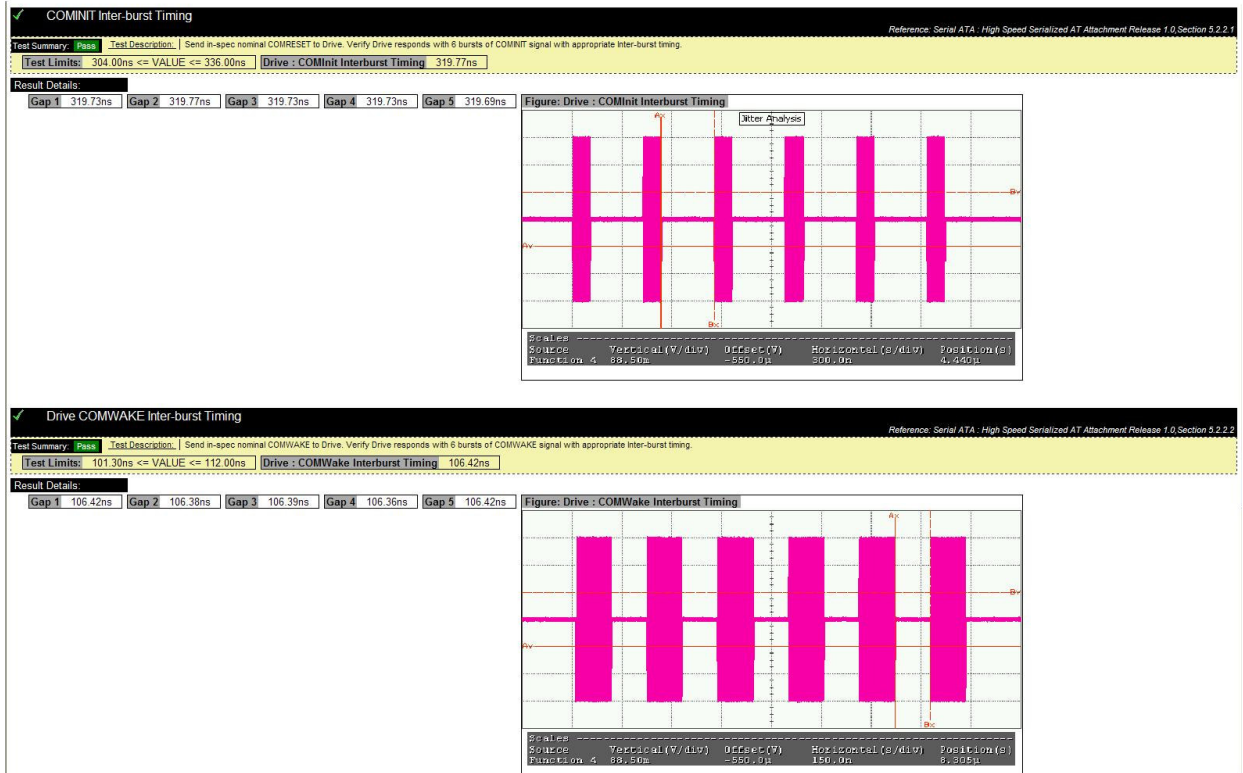
Example N5411A OOB Output Report: This is a section of the HTML output report that illustrates and quantifies the COMINIT and COMWAKE Transmit Gap Lengths.

Possible Problems:

Test OOB-06 – COMWAKE Gap Detection Windows

Purpose: To verify that the COMWAKE Gap Detection Windows of the DUT's receiver are within the conformance limits.

References:
[1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
[2] Ibid, 7.2.2.7.6
[3] Ibid, 7.4.21
[4] SATA Interoperability Program Unified Test Document, 2.14.6 –COMWAKE Gap Detection Windows

Resource Requirements:
Same as for OOB-02.

See Appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the COMWAKE Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the device COMWAKE Gap Detection Windows test in the report generated at the completion of the testing.

Observable Results:
The DUT shall verify COMWAKE detection at the lower limit of 103ns.
The DUT shall verify COMWAKE detection at the upper limit of 110ns.
The DUT shall verify **NO** COMWAKE detection at the lower limit of 30ns.
The DUT shall verify **NO** COMWAKE detection at the upper limit of 177ns.

✓	Drive Responds to max In-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to min In-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects max Out-Of-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects min Out-Of-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to max In-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to min In-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects max Out-Of-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects min Out-Of-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %

Example N5411A OOB Output Report: This section of the N5411A HTML output report that verifies the pass/fail conditions for OOB-06 and OOB-07 detect/reject tests based on the allowed COMWAKE and COMINIT gap times.

Example N5411A OOB Output Report: This section of the N5411A HTML output report that illustrates the pass/fail conditions for OOB-06 and OOB-07 detect/reject tests based on the allowed COMWAKE and COMINIT gap times.

Possible Problems:

NOTE : There is no timing requirement for how soon following a host COMWAKE which the device must respond with a device COMWAKE. For test efficiency purposes, a tester is only required to wait for verification of device COMWAKE up to 100ms following de-qualification of host COMWAKE.

Test OOB-07 – COMINIT Gap Detection Windows

Purpose: To verify that the COMINIT Gap Detection Windows of the DUT's receiver are within the conformance limits.

References:
        [1] SATA Standard, 7.2.1, Table 25 – OOB Specifications
        [2] Ibid, 7.2.2.7.7
        [3] Ibid, 7.4.21
        [4] SATA Interoperability Program Unified Test Document, 2.14.7 – COMINIT Gap Detection Windows

Resource Requirements:
        Same as for OOB-02.

See Appendix A for details.

Last Template Modification: May 7, 2006 (Version 2.01)

Discussion:
        Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the COMINIT Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:
        The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a host or pattern generator will force a hard reset in a device, the following OOB tests can all be performed using an Agilent 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Agilent DSO81204A/B 12GHz oscilloscope, which is running the N5411A SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure device reset, but in some cases, it may still be necessary to remove power from the device under test temporarily to allow the device to exit from a BIST controlled mode and return to normal operation.

Test Procedure:
This parameter is covered by Agilent Technologies, Inc. N5411A automated SATA compliance software, revision 2.01 or later. Either "PASS" or "FAIL" is shown for the device COMINIT Gap Detection Windows test in the report generated at the completion of the testing.

Observable Results:
        The DUT shall verify COMRESET detection at the lower limit of 306ns.
        The DUT shall verify COMRESET detection at the upper limit of 334ns.
        The DUT shall verify **NO** COMRESET detection at the lower limit of 173ns.
        The DUT shall verify **NO** COMRESET detection at the upper limit of 527ns.

✓	Drive Responds to max In-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to min In-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects max Out-Of-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects min Out-Of-Spec COMRESET	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to max In-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Responds to min In-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects max Out-Of-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %
✓	Drive Rejects min Out-Of-Spec COMWAKE	Valid responses / Invalid responses	Valid Responses	0.0 %

Example N5411A OOB Output Report: This section of the N5411A HTML output report that verifies the pass/fail conditions for OOB-06 and OOB-07 detect/reject tests based on the allowed COMWAKE and COMINIT gap times.

Example N5411A OOB Output Report: This section of the N5411A HTML output report that illustrates the pass/fail conditions for OOB-06 and OOB-07 detect/reject tests based on the allowed COMWAKE and COMINIT gap times.

Possible Problems:

NOTE : A device must respond by transmitting COMINIT within 10ms of de-qualification of a received COMRESET signal (see section 8.3.2 of Serial ATA Revision 2.5). With this in mind, a test only needs to wait up to 11ms following de-qualification of COMRESET to ensure that the device is responding. If no COMINIT is received in this timeframe, this is considered a failure by the device to this test.

NOTE : In a case where a device supports Asynchronous Signal Recovery, it is possible that a device may transmit COMINIT pro-actively and not in direct response to a COMRESET. In verification of this test requirement, it is essential that the tester be able to extract any COMINIT response which may be as a result of Asynchronous Signal Recovery, and simply verify COMINIT responses as a result of COMRESET receipt from the host.

Appendix A – Information on Required Resources

Equipment referred to in this document is described here, or references to available resources are cited.

Information on the Agilent DSO81204A/B Infiniium 12GHz real time oscilloscopes and 1169A 12GHz InfiniiMax active voltage probes can be found at:
http://www.agilent.com/find/InfiniiMax2

The N5411A Serial ATA Electrical Performance Validation and Compliance Test Software datasheet and video demonstration can be found at the following URL. The N5411A datasheet contains a list of necessary test connectors and additional hardware/software products in the 'Ordering Information' section for completing the full set of SATA-IO IW PHY, TSG and OOB tests:
http://www.agilent.com/find/n5411a

A picture of the COMAX iSATA(cable connector) to SMA(f) test fixture distributed by CRUZ Systems (H303000204) is shown below for reference. The H303000204 has four SMA(f) connectors labeled 2, 3, 5 & 6. Connectors 2 & 3 relate to device RX+ and RX-, respectively. Connectors 5 & 6 relate to host TX- and TX+, respectively. For more information, or to order a COMAX test fixture distributed by CRUZ Systems, please visit
http://www.CRUZsystems.com

NOTE: The SATA cable end connector on the H303000204 is fragile. Support the cables connected to the H303000204 during connection, testing and disconnect. Do not let their weight be supported by torque on the SATA connector. When unplugging the H303000204 between tests, grasp the sides of the SATA connector, not the semi-rigid coaxial cables mated to the SATA connector. Please also be sure to use (2) 7/16" wrenches when mating and unmating the H303000204 with the 36" SMA cables going to the pattern generator and oscilloscope to ensure that no torque is transferred to the H303000204 cables during testing. The easiest way to set up the cables and test fixture for testing is to loosely connect all SMA connectors to the H303000204 test fixture prior to aligning the SATA connector to the DUT's SATA connector, then tighten the SMA connections using wrenches once the proper alignment of the SATA connectors is achieved. This will prevent damage to the H303000204 test connector, and help to ensure a longer life for this sensitive test fixture.

For OOB transmit timing tests it is necessary for a host to drive the OOB sequence, therefore the host and device must be connected, and the signal must be observed with a (relatively) high impedance differential probe. An adapter must be used to provide access for the probe. This can be done easily with a Crescent Heart Software TF-SATA-IS/XP Interstate Test Fixture, which allows for a high-impedance Agilent 1169A 12GHz Active Differential Voltage Probe Amplifier and E2678A Differential Socketed Probe Head to be connected to the device RX+ and RX-differential pair to observe the differential voltage being applied to the DUT's SATA connector mated pair.

Information about the ULINK Technology, Inc. DriveMaster 2006 software can be obtained from their website at:
http://www.ulinktech.com

**Example N5411A Device Test Initial Setup Procedure**

1. To start the N5411A Application, invoke it from the Analyze->Automated Test Apps->SATA menu tree in the Infiniium Oscilloscope interface.
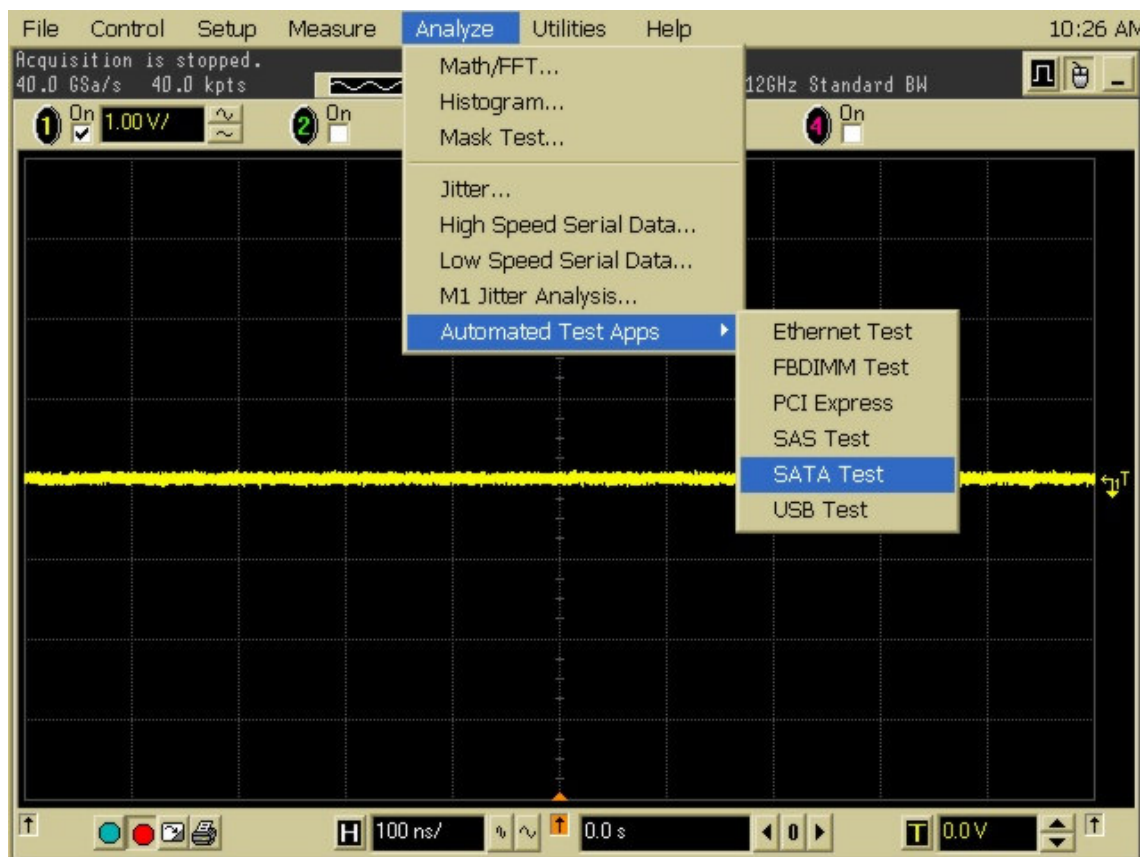
2. Next, choose the type of device that you wish to test (Gen 1i Drive in this example) and associate the 81134A Programmable Pattern Generator LAN connection with the N5411A SATA application.
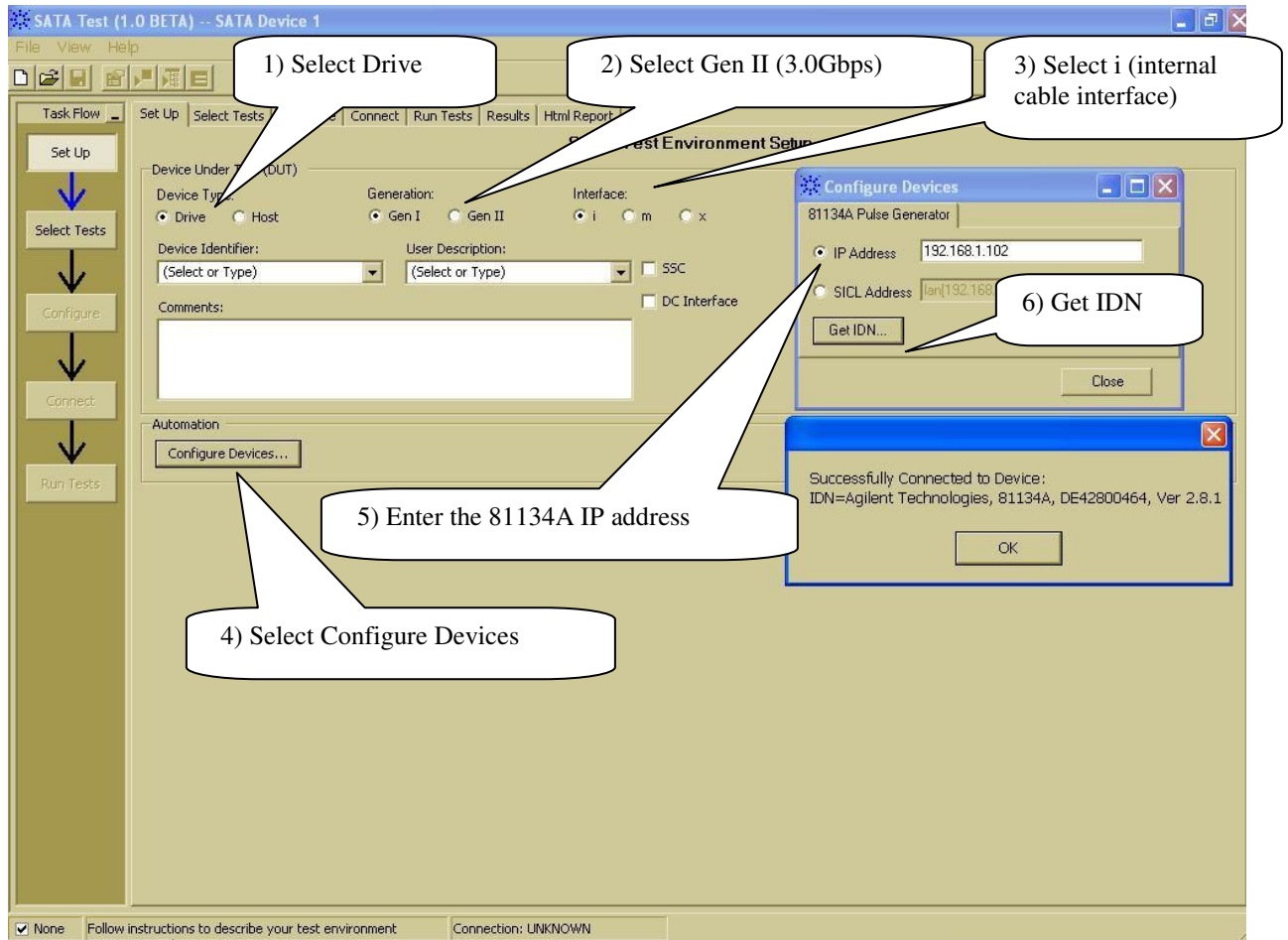
3. Then, click on the "Select Tests" tab and choose the tests that you would like to run. If all tests are desired to be run, then only the top of the main tree needs to be selected. Only the tests for your device/host type and speed are shown in the tree based on your inputs from the previous setup step.
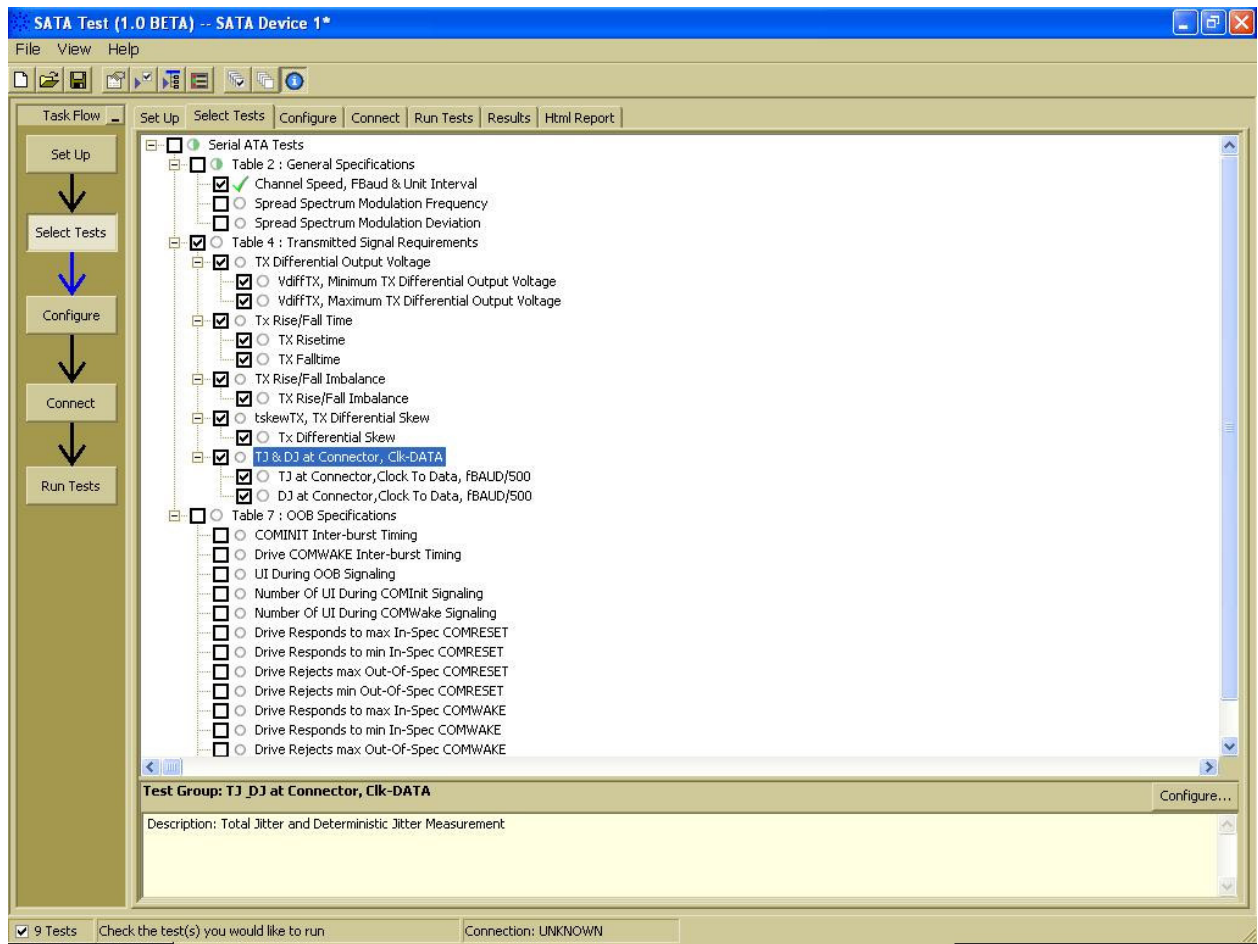
4. Next click on the "Configure Tab" to verify proper setup of the application connection points. The SATA II: Electrical Specification 1.0 currently offers two independent test mode for SATA device or host vendors.
   A. Vendor specific test mode – user must have a method of creating the necessary LFTP, MFTP, HFTP, LBP and SSOP test patterns per the above specification, Sections 6.2.4.3 and 6.4.11. This mode would be selected to support BIST-T,A,S mode and will prompt the user for pattern changes when needed to ensure testing with the correct pattern.
   B. Far-end Retimed Loopback (FERL) mode – REQUIRED for all SATA designs per the above specification, Section 6.2.3. Users will need to enable this FERL feature via a BIST Activate (Bidirectional) FIS command set, with the Loopback (L-bit) asserted. In this mode, the Transmit Only (T-bit), Align bypass (A-bit) and Bypass Scrambling (S-bit) are normally all de-asserted, but will be ignored if the L-bit is asserted. In FERL mode, the 81134A will be programmed to send the required compliance patterns at the appropriate time, thereby automating the user's device/host test solution completely and allowing for simple and quicker test transitions.
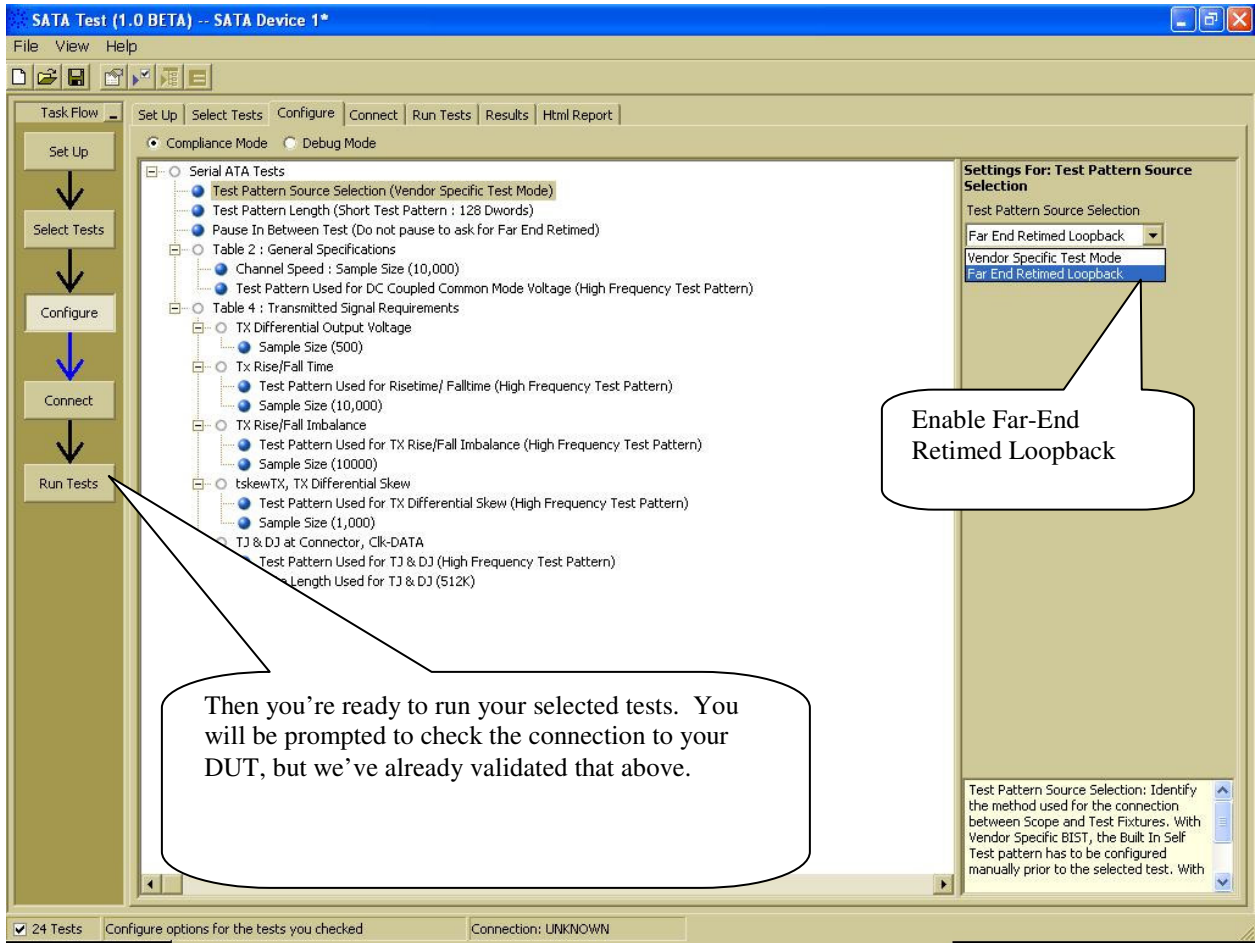
5. Next you will see each one of the tests being performed automatically by the application. A running total of completed tests and a summary of pass/failed tests is also provided. When completed you will see a summary of the test results.

6. Click on the "HTML Report" tab to view a more detailed summary of the testing that includes screen shots taken from the scope.

Agilent Technologies

SATA Test Report

Overall Results: 2 of 9 Tests Failed

Report Style: Compact **Verbose**

Test Configuration Details	
Device Description	
Generation	Gen I
Interface	i
Device Type	Drive
Test Session Details	
Infiniium SW Version	04.21.0000
Infiniium Model Number	DSO81204A
Infiniium Serial Number	No Serial
Last Test Date	10/31/2005 11:20:41 AM

Summary of Results

Margin Thresholds
Warning	< 2 %
Critical	< 0 %

| Pass	Test Name	Spec Range	Measured Value	Margin
✓	Channel Speed, FBaud & Unit Interval	[333.2ps to 335.1ps]	333.3ps	5.3 %
✓	TX Risetime	[67.0ps to 136.0ps]	87.3ps	29.4 %
✓	TX Falltime	[67.0ps to 136.0ps]	86.0ps	27.5 %
✗	TX Rise/Fall Imbalance	<= 20.00%	20.76%	-3.8 %
✓	Tx Differential Skew	<= 20.0ps	10ps	50.0 %
✓	TJ at Connector,Clock To Data, fBAUD/500	<= 370mUI	60mUI	83.8 %
✓	DJ at Connector,Clock To Data, fBAUD/500	<= 190mUI	2mUI	100.0 %

Cable Deskew procedure

This procedure must be performed before measurements are made, and whenever the skew between the positive and negative data input lines may have changed (i.e. cables have been disconnected and reconnected perhaps on the other side of the diff pair). It is always a good practice to allow any real-time oscilloscope or high-performance electronic instrumentation warm-up for at least 20 minutes prior to deskewing channels to allow all critical input circuitry to achieve a steady state at the ambient operating temperature.

Important note: SMA connectors should always be tightened and removed with a calibrated torque wrench designed for that purpose. The torque wrench should limit torque to 5 inch-pounds.

1) Connect one 54855-67604 Precision 7mm (m) to APC 3.5mm (f) adapter each to the inputs of Channel 1 and Channel 3 on the Agilent DSO81204A/B Infiniium Real-time oscilloscope. These adapters will provide SMA connector compatibility at full bandwidth (13GHz) to the front-end of the oscilloscope.

2) Attach one 36" SMA cable (Rosenberger or equivalent) each to the 54855-67604 adapters on the Channel 1 and Channel 3 inputs of the Infiniium scope. Channel 1 will eventually connect to the device TX+ and Channel 3 to the device TX- outputs.
3) Connect any BNC (m) to SMA (m) adapter to the 'Aux Out' connector on the front panel of the Infiniium scope. Now connect the middle input of the Agilent 11636B Power Divider to the SMA connection on the 'Aux Out' connector adapter, which will split the Aux Out signal source into two phase-matched and amplitude balanced outputs.
4) Now attach the SMA cable outputs from Channels 1 & 3 to the remaining two output connections on the Agilent 11636B Power Divider to complete the deskew connection process.
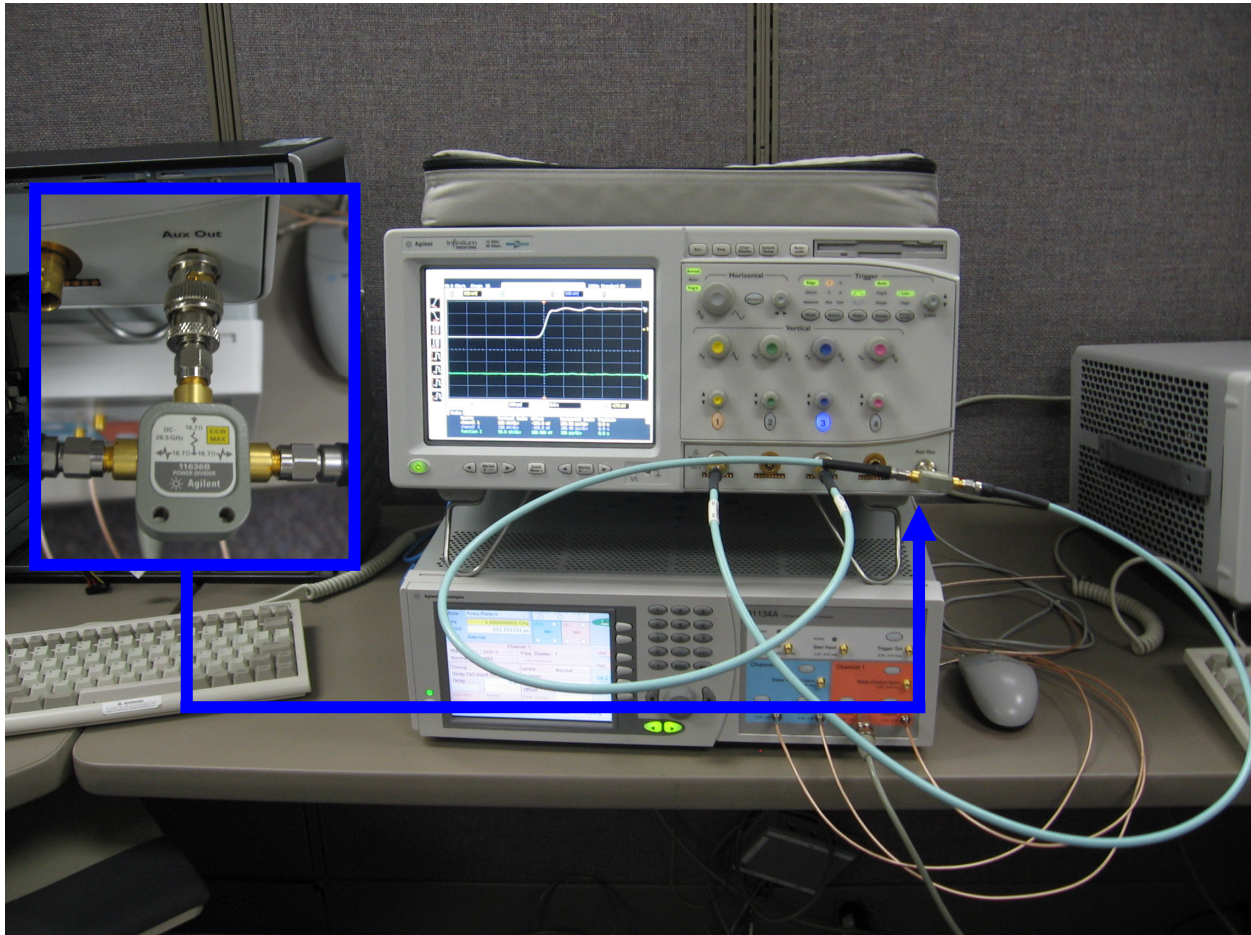
5) Referring to the figure below, perform the following steps.
   a. Select the **File → Load → Setup** menu to open the Load Setup window.
   b. Navigate to the directory location that contains the **INF_SMA_Deskew.set** setup file.
   c. Select the **INF_SMA_Deskew.set** setup file by clicking on it.
   d. Click the **Load** button to configure the oscilloscope from this setup file.
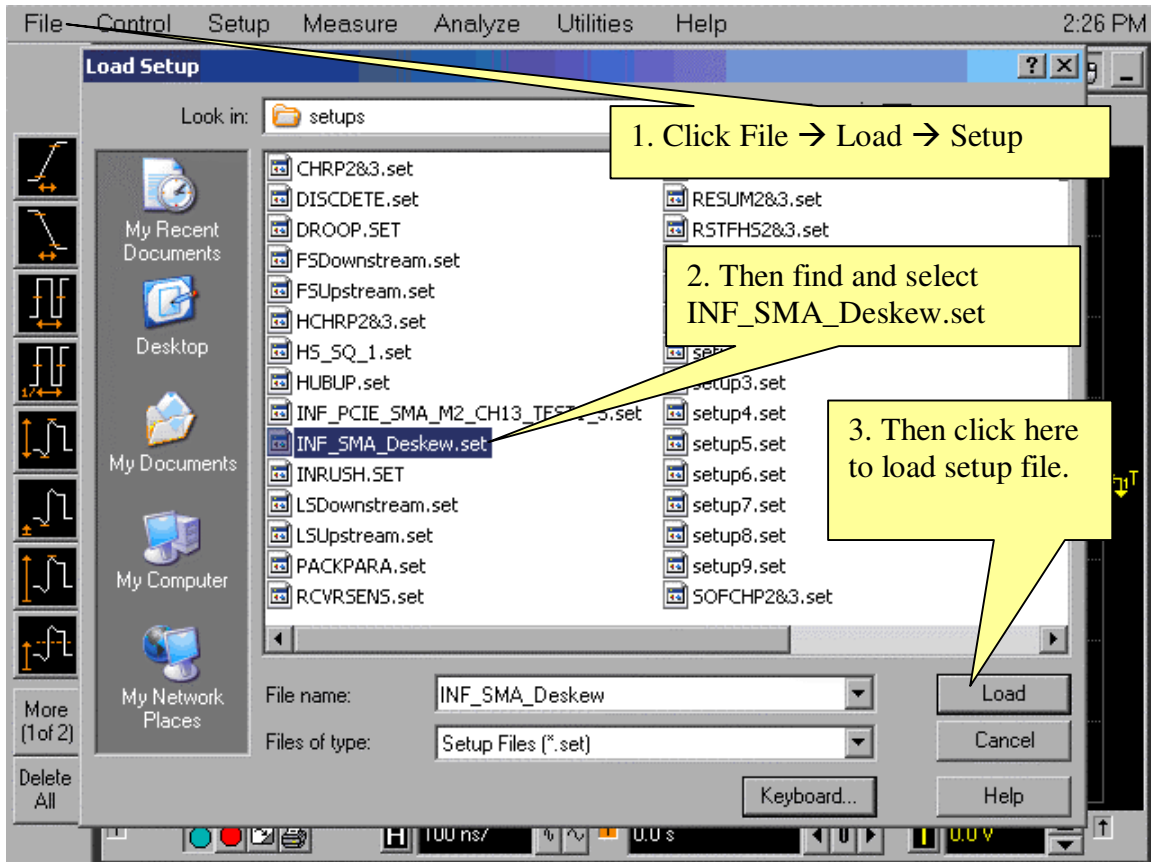
6) If the **INF_SMA_Deskew.set** setup file does not exist, it can be recreated from the following setup configuration on the Infiniium oscilloscope.

INF_SMA_DESKEW.SET setup file details:
Start from a default setup by pressing the **Default Setup** key on the front panel. Then configure the following settings…

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3,
	Vertical scale 50 mV/ Offset 100.000 mV

7) The oscilloscope display should look similar to the figure below. A falling edge of the square wave from Aux Out (approximately a 100ps 20%-80% edge) is shown in a 200ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulting from relative channel skew.

8) Referring to the following figure, perform the following steps to deskew the channels.

    a.   Click on the **Setup → Channel 1** menu to open the **Channel Setup** window.

    b.   Move the **Channel Setup** window to the left so you can see the traces.

    c.   Adjust the Skew by clicking on the ← or → arrows, to achieve the flattest response on the differential signal (green trace).

    d.   Click the Close button on the Channel Setup window to close it.

    e.   The de-skew operation is complete.

    f.   Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

NOTE: Each cable is now deskewed for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to deskew them again. It is recommended that the cables be labeled with the channel they were calibrated for.

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9) The figure below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace) & channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then repeat the steps in section 8 above.

Click Setup → Channel 1 to open the Channel Setup window.

Then adjust the Skew left or right to maximize flatness of green trace.

Then click Close when done.